SAMSUNG

Rev. 1.1, Oct. 2021

M321R2GA3BB0
M321R4GA3BB0
M321R4GA0BB0
M321R8GA0BB0

288pin Registered DIMM based on 16Gb B-die

82FBGA with Lead-Free & Halogen-Free (RoHS compliant)

Datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.5	- Preliminary datasheet.	8th Sep, 2020	Preliminary	J.Y.Lee
0.9	- Update Crosspoint Voltage (VIX) for Differential Input Clock table.	14th Apr, 2021	Preliminary	J.K.Kim J.Y.Kim
0.91	- Bin change(40-40-40 → 40-39-39).	15th Apr, 2021	Preliminary	J.Y.Kim
1.0	- Update Function block diagram.	13th Jul, 2021	Final	J.W.Cho
	- Update IDD and IPP values.			J.Y.Kim
1.01	- KEY FEATURES Typo Correction.	29th Jul, 2021	Final	J.W.Cho
	• Programmable Additive Latency: CL-2 clock → Delete.			J.Y.Kim
	• Programmable CAS Latency (posted CAS) : 26,30,32,36,40,42,46,48,52 → Programmable CAS Latency 22,26,28,30,32,36,40,42.			
	• Programmable CAS Write Latency (CWL) = 32(DDR5-4000), 36(DDR5-4400), 40(DDR5-4800) → Programmable CAS Write Latency (CWL) = RL-2.			
	• CA4 BL*=L -> CA5 BL*=L.			
	- DDR5 Function Matrix			
	• CA parity → Delete.			
	• RFM(V → blank).			
1.02	- Change DDR5 REGISTERED DIMM ORDERING INFORMATION.	5th Aug, 2021	Final	J.W.Cho
	• Organization : 16GB(x80 → 2Gx80). 32GB(x80 → 4Gx80). 32GB(x80 → 4Gx80). 64GB(x80 → 8Gx80).			J.Y.Kim
	• Component Composition : 16GB(16Gbx8 → 2Gx8). 32GB(16Gbx8 → 2Gx8). 32GB(16Gbx8 → 4Gx4). 64GB(16Gbx8 → 4Gx4).			
	• Height : 31mm~32mm → 31.25mm ±0.15mm.			
1.1	- DC Operating Conditions VPP Maximum typo (1.098 → 1.908).	15th Oct, 2021	Final	J.H.Son J.Y.Kim

Table Of Contents

288pin Registered DIMM based on 16Gb B-die

1.0 DDR5 REGISTERED DIMM ORDERING INFORMATION

[Table 1] Ordering Information

Part Number [1)]	Density	Organization	Component Composition[2)]	Number of Rank	Height
M321R2GA3BB0-CQK##	16GB	2Gx80	2Gx8(K4RAH086VB-BCQK) * 10	1	31.25mm±0.15mm
M321R4GA3BB0-CQK##	32GB	4Gx80	2Gx8(K4RAH086VB-BCQK) * 20	2	31.25mm±0.15mm
M321R4GA0BB0-CQK##	32GB	4Gx80	4Gx4(K4RAH046VB-BCQK) * 20	1	31.25mm±0.15mm
M321R8GA0BB0-CQK##	64GB	8Gx80	4Gx4(K4RAH046VB-BCQK) * 40	2	31.25mm±0.15mm

NOTE :
1) "##"- Bucket field for PMIC/RCD information.
2) "QK" - 4400Mbps 36-36-36, 4800Mbps 40-39-39.

2.0 KEY FEATURES

[Table 2] Key Parameters for 4800Mbps Speed Bin

Speed	DDR5-4400	DDR5-4800	Unit
	36-36-36	40-39-39	
tCK(min)	0.454	0.416	ns
CAS Latency	36	40	nCK
tRCD(min)	16.000	16.000	ns
tRP(min)	16.000	16.000	ns
tRAS(min)	32.000	32.000	ns
tRC(min)	48.000	48.000	ns

- JEDEC standard compliant.
- VDD = VDDQ = 1.1V (1.067V(- 3%) ~ 1.166V(+6%)).
- VPP = 1.8V (1.746 (-3%) ~ 1.908 (+6%).
- 2200MHz f_{CK} for 4400Mb/sec/pin, 2400MHz f_{CK} for 4800Mb/sec/pin.
- 32 Banks (8 Bank Groups).
- Programmable CAS Latency (posted CAS): 22,26,28,30,32,36,40,42.
- Programmable CAS Write Latency (CWL) = RL-2.
- 16-bit prefetch.
- Burst Length: 16 by default. 8 with tCCD=8, which does not allow gapless READ or WRITE, where BC8 and BL32 refer to CA5 BL*=L.
- Bi-directional Differential Data-Strobe.
- Internal ZQ calibration via Multi-Purpose Command (MPC) - ZQcal start and ZQcal Latch.
- On Die Termination (ODT) via Mode Register setting : RTT_PARK, RTT_WR, RTT_NOM_WR, RTT_NOM_RD.
- Average Refresh period 3.9us at lower than T_{CASE} 85°C, 1.95us at 85°C < T_{CASE} ≤ 95 °C.
- Connectivity Test Mode (TEN) is supported.
- Asynchronous Reset.

3.0 ADDRESS CONFIGURATION

[Table 3] Address Information

Configuration		4Gb x4	2Gb x8
Bank Address	BG Address	BG0~BG2	BG0~BG2
	Bank Address in a BG	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32
Row Address		R0~R15	R0~R15
Column Address		C0~C10	C0~C9
Page size		1KB	1KB

4.0 REGISTERED DIMM PIN INFORMATION

[Table 4] PIN Configuration

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VIN_BULK	145	VIN_BULK	50	VSS	194	DQ31_A	96	CB0_B	240	VSS
2	RFU	146	VIN_BULK	51	CB0_A	195	VSS	97	VSS	241	CB2_B
3	VIN_MGMT	147	PWR_GOOD/FAIL_n	52	VSS	196	CB2_A	98	CB1_B	242	VSS
4	SCL	148	SAA	53	CB1_A	197	VSS	99	VSS	243	CB3_B
5	SDA	149	RFU	54	VSS	198	CB3_A	100	DQ0_B	244	VSS
6	VSS	150	RFU	55	DQS4_A_t	199	VSS	101	VSS	245	DQ2_B
7	DQ0_A	151	VSS	56	DQS4_A_c	200	DQS9_A_c,TDQS9_A_c	102	DQ1_B	246	VSS
8	VSS	152	DQ2_A	57	VSS	201	DQS9_A_t,TDQS9_A_t	103	VSS	247	DQ3_B
9	DQ1_A	153	VSS	58	CB4_A	202	VSS	104	DQS0_B_t	248	VSS
10	VSS	154	DQ3_A	59	VSS	203	CB6_A	105	DQS0_B_c	249	DQS5_B_c,TDQS5_B_c
11	DQS0_A_t	155	VSS	60	CB5_A	204	VSS	106	VSS	250	DQS5_B_t,TDQS5_B_t
12	DQS0_A_c	156	DQS5_A_c, TDQS5_A_c	61	VSS	205	CB7_A	107	DQ4_B	251	VSS
13	VSS	157	DQS5_A_t, TDQS5_A_t	62	ALERT_n	206	VSS	108	VSS	252	DQ6_B
14	DQ4_A	158	VSS	63	VSS	207	RESET_n	109	DQ5_B	253	VSS
15	VSS	159	DQ6_A	64	CS0_A_n	208	VSS	110	VSS	254	DQ7_B
16	DQ5_A	160	VSS	65	VSS	209	CS1_A_n	111	DQ8_B	255	VSS
17	VSS	161	DQ7_A	66	CA0_A	210	VSS	112	VSS	256	DQ10_B
18	DQ8_A	162	VSS	67	VSS	211	CA1_A	113	DQ9_B	257	VSS
19	VSS	163	DQ10_A	68	CA2_A	212	VSS	114	VSS	258	DQ11_B
20	DQ9_A	164	VSS	69	VSS	213	CA3_A	115	DQS1_B_t	259	VSS
21	VSS	165	DQ11_A	70	CA4_A	214	VSS	116	DQS1_B_c	260	DQS6_B_c,TDQS6_B_c
22	DQS1_A_t	166	VSS	71	VSS	215	CA5_A	117	VSS	261	DQS6_B_t,TDQS6_B_t
23	DQS1_A_c	167	DQS6_A_c,TDQS6_A_c	72	CA6_A	216	VSS	118	DQ12_B	262	VSS
24	VSS	168	DQS6_A_t,TDQS6_A_t	73	VSS	217	CK_t	119	VSS	263	DQ14_B
25	DQ12_A	169	VSS	74	PAR_A	218	CK_c	120	DQ13_B	264	VSS
26	VSS	170	DQ14_A	75	VSS	219	VSS	121	VSS	265	DQ15_B
27	DQ13_A	171	VSS	KEY				122	DQ16_B	266	VSS
28	VSS	172	DQ15_A					123	VSS	267	DQ18_B
29	DQ16_A	173	VSS					124	DQ17_B	268	VSS
30	VSS	174	DQ18_A	76	CA0_B	220	RFU	125	VSS	269	DQ19_B
31	DQ17_A	175	VSS	77	VSS	221	CA1_B	126	DQS2_B_t	270	VSS
32	VSS	176	DQ19_A	78	CA2_B	222	VSS	127	DQS2_B_c	271	DQS7_B_c,TDQS7_B_c
33	DQS2_A_t	177	VSS	79	VSS	223	CA3_B	128	VSS	272	DQS7_B_t,TDQS7_B_t
34	DQS2_A_c	178	DQS7_A_c,TDQS7_A_c	80	CA4_B	224	VSS	129	DQ20_B	273	VSS
35	VSS	179	DQS7_A_t, TDQS7_A_t	81	VSS	225	CA5_B	130	VSS	274	DQ22_B
36	DQ20_A	180	VSS	82	CA6_B	226	VSS	131	DQ21_B	275	VSS
37	VSS	181	DQ22_A	83	VSS	227	PAR_B	132	VSS	276	DQ23_B
38	DQ21_A	182	VSS	84	CS0_B_n	228	VSS	133	DQ24_B	277	VSS
39	VSS	183	DQ23_A	85	VSS	229	CS1_B_n	134	VSS	278	DQ26_B
40	DQ24_A	184	VSS	86	LBD, RSP_A_n	230	VSS	135	DQ25_B	279	VSS
41	VSS	185	DQ26_A	87	LBS, RSP_B_n	231	RFU	136	VSS	280	DQ27_B
42	DQ25_A	186	VSS	88	VSS	232	RFU	137	DQS3_B_t	281	VSS
43	VSS	187	DQ27_A	89	CB4_B	233	VSS	138	DQS3_B_c	282	DQS8_B_c,TDQS8_B_c
44	DQS3_A_t	188	VSS	90	VSS	234	CB6_B	139	VSS	283	DQS8_B_t,TDQS8_B_t
45	DQS3_A_c	189	DQS8_A_c,TDQS8_A_c	91	CB5_B	235	VSS	140	DQ28_B	284	VSS
46	VSS	190	DQS8_A_t, TDQS8_A_t	92	VSS	236	CB7_B	141	VSS	285	DQ30_B
47	DQ28_A	191	VSS	93	DQS9_B_t, TDQS9_B_t	237	VSS	142	DQ29_B	286	VSS
48	VSS	192	DQ30_A	94	DQS9_B_c,TDQS9_B_c	238	DQS4_B_c	143	VSS	287	DQ31_B
49	DQ29_A	193	VSS	95	VSS	239	DQS4_B_t	144	RFU	288	VSS

Front Side Pin Label	Pin	Pin	Back side Pin Label
VIN_BULK	1	145	VIN_BULK
RFU	2	146	VIN_BULK
VIN_MGMT	3	147	PWR_GOOD/FAIL_n
HSCL	4	148	HSA
HSDA	5	149	RFU
VSS	6	150	RFU
DQ0_A	7	151	VSS
VSS	8	152	DQ2_A
DQ1_A	9	153	VSS
VSS	10	154	DQ3_A
DQS0_A_t	11	155	VSS
DQS0_A_c	12	156	DQS5_A_c, TDQS5_A_c
VSS	13	157	DQS5_A_t, TDQS5_A_t DBI0_A_n
DQ4_A	14	158	VSS
VSS	15	159	DQ6_A
DQ5_A	16	160	VSS
VSS	17	161	DQ7_A
DQ8_A	18	162	VSS
VSS	19	163	DQ10_A
DQ9_A	20	164	VSS
VSS	21	165	DQ11_A
DQS1_A_t	22	166	VSS
DQS1_A_c	23	167	DQS6_A_c, TDQS6_A_c
VSS	24	168	DQS6_A_t, TDQS6_A_t DBI1_A_n
DQ12_A	25	169	VSS
VSS	26	170	DQ14_A
DQ13_A	27	171	VSS
VSS	28	172	DQ15_A
DQ16_A	29	173	VSS
VSS	30	174	DQ18_A
DQ17_A	31	175	VSS
VSS	32	176	DQ19_A
DQS2_A_t	33	177	VSS
DQS2_A_c	34	178	DQS7_A_c, TDQS7_A_c
VSS	35	179	DQS7_A_t, TDQS7_A_t DBI2_n
DQ20_A	36	180	VSS
VSS	37	181	DQ22_A
DQ21_A	38	182	VSS

Front Side Pin Label	Pin	Pin	Back side Pin Label
PAR_A	74	218	CK_c
VSS	75	219	VSS
	Key		
CA0_B	76	220	RFU
VSS	77	221	CA1_B
CA2_B	78	222	VSS
VSS	79	223	CA3_B
CA4_B	80	224	VSS
VSS	81	225	CA5_B
CA6_B	82	226	VSS
VSS	83	227	PAR_B
CS0_B_n	84	228	VSS
VSS	85	229	CS1_B_n
LBD, RSP_A_n	86	230	VSS
LBS, RSP_B_n	87	231	RFU
VSS	88	232	RFU
CB4_B	89	233	VSS
VSS	90	234	CB6_B
CB5_B	91	235	VSS
VSS	92	236	CB7_B
DQS9_B_t, TDQS9_B_t. DBI4_B_n	93	237	VSS
DQS9_B_c, TDQS9_B_c.	94	238	DQS4_B_c
VSS	95	239	DQS4_B_t
CB0_B	96	240	VSS
VSS	97	241	CB2_B
CB1_B	98	242	VSS
VSS	99	243	CB3_B
DQ0_B	100	244	VSS
VSS	101	245	DQ2_B
DQ1_B	102	246	VSS
VSS	103	247	DQ3_BDQ3_B
DQS0_B_t	104	248	VSS
DQS0_B_c	105	249	DQS5_B_c, TDQS5_B_c
VSS	106	250	DQS5_B_t, TDQS5_B_t DBI0_B_n
DQ4_B	107	251	VSS
VSS	108	252	DQ6_B
DQ5_B	109	253	VSS

Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	39	183	DQ23_A
DQ24_A	40	184	VSS
VSS	41	185	DQ26_A
DQ25_A	42	186	VSS
VSS	43	187	DQ27_A
DQS3_A_t	44	188	VSS
DQS3_A_c	45	189	DQS8_A_c, TDQS8_A_c
VSS	46	190	DQS8_A_t, TDQS8_A_t DBI3_A_n
DQ28_A	47	191	VSS
VSS	48	192	DQ30_A
DQ29_A	49	193	VSS
VSS	50	194	DQ31_A
CB0_A	51	195	VSS
VSS	52	196	CB2_A
CB1_A	53	197	VSS
VSS	54	198	CB3_A
DQS4_A_t	55	199	VSS
DQS4_A_c	56	200	DQS9_A_c, TDQS9_A_c
VSS	57	201	DQS9_A_t, TDQS9_A_t DBI4_A_n
CB4_A	58	202	VSS
VSS	59	203	CB6_A
CB5_A	60	204	VSS
VSS	61	205	CB7_A
ALEFT_n	62	206	VSS
VSS	63	207	RESET_n
CS0_A_n	64	208	VSS
VSS	65	209	CS1_A_n
CA0_A	66	210	VSS
VSS	67	211	CA1_A
CA2	68	212	VSS
VSS	69	213	CA3_A
CA4_A	70	214	VSS
VSS	71	215	CA5_A
CA6_A	72	216	VSS
VSS	73	217	CK_t

Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	110	254	DQ7_B
DQ8_B	111	255	VSS
VSS	112	256	DQ10_B
DQ9_B	113	257	VSS
VSS	114	258	DQ11_B
DQS1_B_t	115	259	VSS
DQS1_B_c	116	260	DQS6_B_c, TDQS6_B_c
VSS	117	261	DQS6_B_t, TDQS6_B_t DBI1_B_n
DQ12_B	118	262	VSS
VSS	119	263	DQ14_B
DQ13_B	120	264	VSS
VSS	121	265	DQ15_B
DQ16_B	122	266	VSS
VSS	123	267	DQ18_B
DQ17_B	124	268	VSS
VSS	125	269	DQ19_B
DQS2_B_t	126	270	VSS
DQS2_B_c	127	271	DQS7_B_c, TDQS7_B_c
VSS	128	272	DQS7_B_t, TDQS7_B_t DBI2_B_n
DQ20_B	129	273	VSS
VSS	130	274	DQ22_B
DQ21_B	131	275	VSS
VSS	132	276	DQ23_B
DQ24_B	133	277	VSS
VSS	134	278	DQ26_B
DQ25_B	135	279	VSS
VSS	136	280	DQ27_B
DQS3_B_t	137	281	VSS
DQS3_B_c	138	282	DQS8_B_c, TDQS8_B_c
VSS	139	283	DQS8_B_t, TDQS8_B_t DBI3_B_n
DQ28_B	140	284	VSS
VSS	141	285	DQ30_B
DQ29_B	142	286	VSS
VSS	143	287	DQ31_B
RFU	144	288	VSS

Figure 1. Wiring Assignments

NOTE :

1) Individual Annex Specifications for RDIMM define pin use where multiple functions are possible.

[Table 5] PIN Description

Pin Name	Description
CA[6:0]_A CA[6:0]_B	SDRAM Address and Command Bus
CS[1:0]_A CS[1:0]_B	SDRAM Chip Select
PAR_A PAR_B	SDRAM Parity input
CK_t	SDRAM Clocks (true/positive)
CK_c	SDRAM Clocks (complement/negative)
ALERT_n	SDRAM alert for CRC error
RESET_n	Set DRAM to known state
PCAMP	Control and Monitor Port
HSCL	I2C/I3C-Basic Host Sideband Bus Clock
HSDA	I2C/I3C-Basic Host Sideband Bus Data
HSA	I2C/I3C-Basic Host Sideband Bus Address
LBDQ	Loopback data output:

Pin Name	Description
DQ[31:0]_A DQ[31:0]_B	DIMM memory data bus channel A and B
CB[7:0]_A CB[7:0]_B	DIMM ECC check bits(CB) channel A and B
DQS[9:0]_A_t DQS[9:0]_B_t	SDRAM data strobes (positive line of differential pair)
DQS[9:0]_A_c DQS[9:0]_B_c	SDRAM data strobes (negative line of differential pair)
TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
VIN_BULK	DIMM Power Supply from system to PMIC
VIN_MGMT	DIMM Power Supply from system to PMIC
VSS	Power supply return (ground)
RFU	Reserved for future use
LBDQS	Loopback data strobe output

NOTE :
1) TDQSx and DQSx_t share a pin.

5.0 THERMAL SENSOR INFORMATION

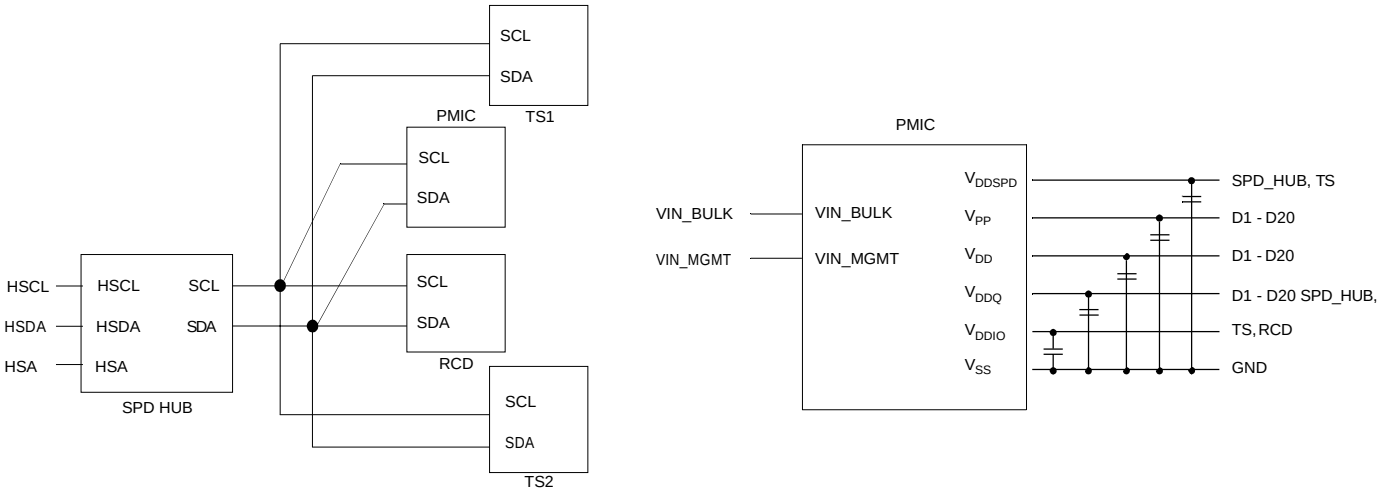


Figure 2. Block Diagram for Thermal Sensor

[Table 6] Thermal Sensor Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions
Temperature Sensor Accuracy (Active Range)	-	0.5	1.0	ºC	75ºC ≤ T_A ≤ 95ºC 40ºC ≤ T_A ≤ 125ºC −40ºC ≤ T_A ≤125ºC
Temperature Sensor Accuracy (Industrial Temperature Range)	-	2.0	3.0	ºC	
Resolution		0.25		ºC	
Conversion Time			125	ms	Assumes 0.25 accuracy
Hysteresis between temperature events	1	-	-	ºC	

6.0 INPUT/OUTPUT FUNCTIONAL DESCRIPTION

[Table 7] Input/Output Function Description

Symbol	Type	I/O Levels	Function
CS[1:0]_A CS[1:0]_B	Input	VDD	Chip Select : All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and VREF parameters as configured by the CA_ODT strap setting or mode register. When in self refresh the CS_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
PAR_A PAR_B	Input	VDD	Command and Address Parity Input: DDR5 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CSx_x_n LOW
ALERT_n	Output	VDD	Alert : If there is an error in CRC, then ALERT_n shall drive LOW for the period time interval and return HIGH. During Connectivity Test mode, this pin functions as an input. Usage of this signal or not is system-dependent. In case this pin is not connected, ALERT_n pin must be bonded to VDDQ on the system board.
RESET_n	CMOS Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.
PCAMP	Input Output	3.6V(max)	Control and Monitor Port. Provides three different functions: (1) Register write protect function; (2) Fail_n function; and (3) Status function (PWR_GOOD).
HSCL	Input	VOUT_1.0 V	Bus clock used to strobe data into HUB device. When open drain, a pullup resistor is required on the system motherboard.
HSDA	Input/ Output	VOUT_1.0 V	I2C/I3C-Basic data. When Open drain, a pullup resistor is required on the system motherboard.
HSA	Input	2.1V max	Device address for the HUB. Tied to GND through resistor for HID in normal operation and directly to GND in tester operation
DQ[31:0]_A DQ[31:0]_B	Input/ Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
CB[7:0]_A CB[7:0]_B	Input/ Output	VDD	ECC Check Bits Input/ Output: Bi-directional data bus.
DQS[9:0]_A_t DQS[9:0]_B_t DQS[9:0]_A_c DQS[9:0]_B_c	Input/ Output	VDD	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
TDQS[9:5]_A_t TDQS[9:5]_B_t TDQS[9:5]_A_c TDQS[9:5]_B_c	Input	VDD	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs.
LBDQ	Output	VDDQ	Loopback data output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled the pin is either terminated or Hi-Z based on MR36:OP[2:0].
LBDQS	Output	VDDQ	Loopback data strobe output: This is a single ended strobe with the rising edged aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled it is in driver mode using the default RON described in the Loopback function section. When Loopback is disabled, the pin is either terminated or Hi-Z based on MR36:OP[2:0].
RFU			Reserved for Future Use: No on DIMM electrical connection is present.

[Table 7] Input/Output Function Description

Symbol	Type	I/O Levels	Function
VIN_BULK	Supply		External power supply: 12V, 4.25V (min), 15V (max)
VIN_MGMT	Supply		External power supply: 3.3V, 3.0V (min), 3.6V (max)
VSS	Supply		Ground

7.0 REGISTERING CLOCK DRIVER SPECIFICATION

7.1 Input Timing Requirement

[Table 8] Input Timing Requirements

Symbol	Parameter	Conditions	DDR5-4400		DDR5-4800		Unit	Note
			Min	Max	Min	Max		
f_{CLOCK}	Input clock frequency	Application frequency	1400	2436	1400	2436	MHz	1,2
f_{TEST}	Input clock frequency	Test frequency	140	1400	140	1400	MHz	3
t_{MRD}	Control word to control word delay	Number of clock cycles between two control word accesses or one control word access and any DRAM command.	8	-	8	-	t_{CK}	
t_{MRD_L}	Control word to control word delay	Number of clock cycles between an access to RW0A, RW0B, RW0C, RW0D,RW10, RW25, RW26, RW27, RW31[7:2], RW[4B:40], RW5E, RW5F ,PG[1:0]RW[7C:61] (i.e., any receiver DFE tap coefficient value) and the next control word access or DRAM command.	16	-	16	-	t_{CK}	4,5,6
t_{MRD_L2}	Control word to control word delay	Number of clock cycles between an access to RW00, RW01, RW02, RW03,RW05, RW06, RW07, RW09, RW0E, RW0F, RW11[2:0], RW32[7:6,2:1] and the next control word access or DRAM command.	32	-	32	-	t_{CK}	7,8,9
t_{MRD_L3}	Control word to control word delay for DFE Gain Adjustment	Waiting time between an access to RW32[5:3,0], PG[1:0]RW[60,68,70,78] and the next input DCS_n assertion	300		300		ns	
t_{MRD_L4}	Control word to control word delay for DFE Vref Settling Time	Waiting time between an access to RW31[1:0], RW3F, PG02RW[62,66,6A,6E,72,76,7A,7E] and the next input DCS_n assertion.	300	-	300	-	ns	
t_{MRC}	Register command word to CW or DRAM command delay.	Number of clock cycles between register command word(RW04) and CW or any DRAM command.	32	-	32	-	t_{CK}	
$t_{Ext\_L-B\_Entry}$	External Loopback Entry Time	Delay from MRW(RW26) that enables External Loopback and start of valid QLBD/QLBS forwarded from selected DLBD/DLBS.	-	300	-	300	ns	
t_{MRD2N}	Control word to control word delay in SDR/2N mode.	Number of clock cycles between two control word accesses or one control word access and any DRAM command.	16	-	16	-	t_{CK}	
t_{MRD2N_L}	Control word to control word delay in SDR/2N mode.	Number of clock cycles between an access to RW0A, RW0B, RW0C, RW0D, RW10, RW25, RW26, RW27, RW[4B:40], RW5E, RW5F and the next control word access or DRAM command.	24	-	24	-	t_{CK}	4,5,6
t_{MRD2N_L2}	Control word to control word delay in SDR/2N mode.	Number of clock cycles between an access to RW00, RW01, RW02, RW03, RW05, RW06, RW07, RW09, RW0E, RW0F, RW11[2:0], RW32[7:6,2:1] and the next control word access or DRAM command.	50	-	50	-	t_{CK}	7,8,9

Symbol	Parameter	Conditions	DDR5-4400		DDR5-4800		Unit	Note
			Min	Max	Min	Max		
t_{MRC2N}	Register command word to CW or DRAM command delay in SDR/2N mode.	Number of clock cycles between register command word(RW04) and CW or any DRAM command.	40	-	40	-	t_{CK}	
$t_{RWUPDInit}$	Time needed from enter into RWUPD to being able to receive in band RW updates		150	-	150	-	ns	
$t_{RWUP-DA2D}$	Time between address transfer and data transfer		8	-	8	-	t_{CK}	
$t_{RWUPDD2A}$	Time between data transfer and next operation address transfer		8	-	8	-	t_{CK}	
$t_{RWUP-DExit}$	Time needed between last RWUPD CS1_n de-assertion and the first CS0_n assertion of DFE training mode or any other operation		150	-	150	-	ns	10
t_{DSCT-M_Entry}	Registration of DCSTM entry from SMBus RW command to start of training samples time		-	250	-	250	ns	
t_{DSCT-M_Exit}	Registration of DCSTM exit from SMBus RW command to end of training mode		-	250	-	250	ns	
t_{DSCT-M_Valid}	Time from sample evaluation to output on ALERT_n or QLBx		-	20	-	20	t_{CK}	
$t_{DSCTM\_ALERT\_Window}$	Time output is available on ALERT_n or OLBx		2	-	2	-	t_{CK}	11
t_{QCST-M_Entry}	Registration of QCSTM entry from MRW command to start QCS training pattern		-	72	-	72	t_{CK}	
t_{QCST-M_Exit}	Registration of QCSTM exit from SMBus RW command to end of QCS training pattern		-	72	-	72	t_{CK}	
t_{DCAT-M_Entry}	Registration of DCATM entry from SMBus RW command to start of training samples time		-	250	-	250	ns	
t_{DCAT-M_Exit}	Registration of DCATM exit from SMBus RW command to end of training mode		-	250	-	250	ns	12
$t_{DCAT-M\_CS\_Exit}$	Time DSC0_n must be held LOW to exit from DCATM training mode		2	8	2	8	t_{CK}	12
t_{DCAT-M_Valid}	Time from sample evaluation to output on ALERT_n or QLBx		-	20	-	20	t_{CK}	
$t_{DCATM\_ALERT\_Window}$	Time output is available on ALERT_n or QLBx		2	-	2	-	t_{CK}	11
$t_{DFETM\_Interval}$	Number of cycles for CA DFE Training data comparison for each output result.		4	4	4	4	t_{CK}	
t_{DFET-M_Valid}	Time from end of CA DFE Training data comparison to valid result output.		-	20	-	20	t_{CK}	
$t_{DFETM\_RSP\_Window}$	Duration of CA DFE Training output result signal pulse.		2	-	2	-	t_{CK}	

Symbol	Parameter	Conditions	DDR5-4400		DDR5-4800		Unit	Note
			Min	Max	Min	Max		
$t_{DFET-M\_Pattern\_Wait\_Accel}$	Time between de-assertion of DSC0_n for one pattern to DCS0_n assertion of the next pattern.	DFE Training Accelerator enabled.	64	-	64	-	t_{CK}	13
$t_{DFET-M\_Pattern\_Wait}$	Time between de-assertion of DSC0_n for one pattern to DCS0_n assertion of the next pattern.	DFE Training Accelerator disabled.	16	-	16	-	t_{CK}	14
t_{CSALT}	Chip select assertion before and after ALERT_n Pulse Width deassertion	Number of clock cycles between DSCx assertion and rising edge of ALERT_n when RW01[6] = 1	8	-	8	-	t_{CK}	
t_{CPDED}	Minimum time between SRE and DSC pluse to drive QCS LOW.	DSC[1:0]_n = HIGH; DRST_n=HIGH; DCK_t/DCT_c=Toggling	Min:max(8nCK,5ns);Max:(-)		Min:max(8nCK,5ns);Max:(-)		t_{CK}	
t_{PDEX}	Minimum time between PDE and PDX in the same rank.		Min:max(16nCK,10ns);Max:(-)		Min:max(16nCK,10ns);Max:(-)		t_{CK}	
t_{RPDX}	Minimum time between RCD PDX and the next valid command other than DRAM Exit from PD		Min:max(16nCK,10ns);Max:(-)		Min:max(16nCK,10ns);Max:(-)		t_{CK}	15
$t_{CPD-ED2SRX}$	Minimum time from single DCS LOW pulse following SRE command to NOP(SRX) command	DSC[1:0]_n=LOW; DRST_n=HIGH	Min:max(16nCK,10ns);Max:(-)		Min:max(16nCK,10ns);Max:(-)		t_{CK}	
t_{CSSR}	Minimum DCS[1:0]_n LOW time (after SRE) when entering DCK stop	DSC[1:0]_n=LOW;DRST_n=HIGH;DCK_t/DCK_c invalid	Min:max(24nCK,15ns);Max:(-)		Min:max(24nCK,15ns);Max:(-)		t_{CK}	
t_{CKoff}	Minimum time required after DSC[1:0]_n goes LOW following SRE command to DCK stop	DSC[1:0]_n=LOW;DRST_n=HIGH;DCK_t/DCK_c Toggling	Min:max(24nCK,15ns);Max:(-)		Min:max(24nCK,15ns);Max:(-)		t_{CK}	
$t_{SRX2SRX}$	Minimum number of valid input clock cycles between SRX command to release QCS and SRX to take DRAM out of Self Refresh	DB control interface disabled (RW09[3]=0)	Min:max(16nCK,10ns);Max:(-)		Min:max(16nCK,10ns);Max:(-)		t_{CK}	
t_{DFD_PRD}	Minimum time from static HIGH or Valid DCA[6:0]/DPAR before initial DSC_n assertion	DFE Enabled during Reset with Stable Power or Self Refresh Exit			Min:max(8nCK,5ns);Max:(-)		t_{CK}	
$t_{DCSL-HSK1}$	Maximum delay between any DSCx_n in LOW-to-HIGH transition from Initialization or Exit from Self Refresh With Clock Stop		200		200		ns	
$t_{DCSL-HSK2}$	Maximum delay between DSC0_n and DSC1_n (within the same sub-channel) in LOW-to-HIGH transition form Initialization or Exit from Self Refresh With Clock Stop		500		500		ps	
t_{XS}	DRAM Exit Self Refresh to next valid command not requiring DLL		See DDR5 DRAM Specification		See DDR5 DRAM Specification			
t_{RINIT1}	Minimum DRST_n LOW time after completion of voltage ramp		200	-	200	-	us	
	Minimum DRST_n LOW time with stable power		1	-	1	-	us	
t_{RINIT2}	Min DCS_n LOW time to DRST_n HIGH		20	-	20	-	ns	
t_{RINIT3}	Minimum DCS_n LOW time after DRST_n HIGH		20	-	20	-	ns	

Symbol	Parameter	Conditions	DDR5-4400		DDR5-4800		Unit	Note
			Min	Max	Min	Max		
t_{CKACT}	Maximum time from DSC_n transition HIGH to start of valid DCK		-	16	-	16	t_{CK}	
t_{XPR}	DRAM minimum time from Exit Reset to first valid Configuration Command		Min(max(5nCK,t_{RFC}(min)+10ns);Max:(-), See DDR5 DRAM Specification		Min(max(5nCK,t_{RFC}(min)+10ns);Max:(-), See DDR5 DRAM Specification		ns	
t_{ZQCAL}	ZQ Calibration Time		1	-	1	-	us	
t_{ZQLAT}	ZQ Calibration Latch Time		Min(max(30ns,8nCK);Max:(-)		Min(max(30ns,8nCK);Max:(-)		ns	

NOTE :

1) Including SSC according Table 197(JESD82-511), "SSC and PLL Loop Filter Characteristics"
2) All specified timing parameters apply
3) Timing parameters specified for frequency band 2 apply
4) Since RW0A, RW0B,RW0C,RW0D affect output driver operation, it is necessary for these setting to be updated during initialization when Bits OP[1] and OP[3] in RCD control word RW01 are still configured to block all commands at the DRAM and Data Buffer interfaces, respectively
5) When Vref settings for DLBD, DLBS, DERROR_IN_n, DCA[6:0], DPAR and DCS[1:0]_n are updated, it is necessary to meet the Vref settling times defined in Table 192(JESD82-511) in addition to meeting t_{MRD_L}
6) Applies to the timing between MRW to RW5E or RW5F in RCD space and MRW to MR63 in DRAM space only during an RCD Control Word Read sequence, otherwise this parameter does not apply to RW5E or RW5F
7) A t_{STAB} waiting time is required when changing the setting in RW00[0] (Command Address SDR/DDR Rate selection), RW05[3:0](RDIMM Operating Speed), RW05[7](Frequency Band Select), and RW06(Fine Granularity Operation Speed)
8) When exiting from RW In-Band Update mode(i.e, when writing a 1 to RW32[7]), it is necessary to meet the $t_{RWUPDExit}$ timing parameter defined in Table 8 in addition to meeting t_{MRD_L2}
9) This parameter also applies to control words inside the DDR5DB01 device. Refer to JESD82-521 for details
10) This parameter also covers the exit latency if exit is triggered through SMBus operation
11) As shown in Figure 119(JESD82-511), this is the minimum guaranteed LOW pulse (i.e., below[V_{OH}+V_{OL}]/2, where V_{OH} and V_{OL} are the measured Logic HIGH and LOW DC voltage levels) into the test load. Logically, the minimum pulse width out of the RCD in DCS or DCA training modes is four DCK clock cycles wide
12) For the double CS Exit the corresponding Host Interface TM selection in RW02 will be reset to default (Normal Operating Mode)
13) When the DFE Training Acceleration is enabled, the minimum waiting time between de-assertion of DCS0_n for one pattern and assertion of DSC0_n of the next pattern is determined by the larger of tDFETM_Pattern_Wait_Accel [min] specified in this table and the minimum settling time for the parameter setting updated by the Training Accelerator logic (e.g. for DFE_Vref or VrefCA, the minimum settling time could be much larger than tDFETM_Pattern_Wait_Accel [mim])
14) When the DFE Training Acceleration is disabled, there is a different minimum spacing between patterns, since there is no need to account for automated parameter changes
15) During the t_{RPDX} window, the logic levels for QACA[13:0] and QBCA[13:0] outputs are not deterministic as the RCD transitions from disabled DCA[6:0]&DPAR receivers to normal operation. During this time, the host is allowed to take a memory rank still in PDE out of power-down state using one DCS_n pulse, but it must refrain from sending any additional commands to any memory rank that has already received its first PDX CS_n pulse. By the end of the t_{RPDX} window, the DDR5RCD01 device is required to forward any legal command from the DCA[6:0] inputs to the QxCA[13:0] and BCOM[2:0] out puts as defined in normal operation requirements

7.2 Output Timing Requirements

[Table 9] Output Timing Requirements

Symbol	Parameter	Conditions	DDR5-4400		DDR5-4800		Unit	Note
			Min	Max	Min	Max		
t_{PDM}	Propagation delay, single bit switching; DCK_t/DCK_c falling edge crosspoint to output	1.1V Operation, DDR Mode (RW00[0]=1)	0.95	1.25	0.95	1.25	ns	2
t_{PDM2N}	Propagation delay, single bit switching; DCK_t/DCK_c rising edge crosspoint to output	1.1V Operation, SDR Mode (RW00[0]=0)	0.95	1.25	0.95	1.25	ns	3
t_{PDM_LB}	Propagation delay; External Loop-back signals	1.1V Operation	-	2	-	2	ns	4
tQLBSL	Loopback QLBS Output Low Time	1.1V Operation, DDR Mode (RW00[0]=1)	TBD	-	TBD	-	t_{CK}	5
tQLBSH	Loopback QLBS Output High Time	1.1V Operation, DDR Mode (RW00[0]=1)	TBD	-	TBD	-	t_{CK}	5
tQLBS2Q	Loopback QLBS to QLBD Skew	1.1V Operation	-	0.15	-	0.15	t_{CK}	
tQLBDH	Loopback QLBD Output Hold Time	1.1V Operation, DDR Mode (RW00[0]=1)	TBD	-	TBD	-	t_{CK}	5
tQLBDVW	Loopback QLBD Valid Window (tQLBDH-tQLBS2Q)	1.1V Operation, DDR Mode (RW00[0]=1)	TBD	-	TBD	-	t_{CK}	5
tDCK2QLBS	Internal Loopback Propagation Delay from Rising (RW26[7]=0) or Falling (RW26[7]=1) DCK crossing point to the Corresponding QLBS Rising Edge.	1.1V Operation, DDR Mode (RW00[0]=1)	-	10	-	10	t_{CK}	5
t_{QSK}	Total magnitude of Qn Output to Output Clock tolerance within the same A or B group (in the same unit) $t_{QSK} = t_{QSK\_static} + t_{QSK\_dynamic}$	Across the supported voltage-temperature range and with SSO conditions and pattern dependence included	0	0.385	0	0.385	t_{CK}	6,7
t_{QSK_static}	Magnitude of Qn Output to Output Clock tolerance within the same A or B group (in the same unit) under quiet conditions	Measured with quiet conditions, only one output switching, and nominal V-T conditions of V_{DD}=1.1V and 25℃	0	0.3	0	0.3	t_{CK}	7,8
$t_{QSK\_dynamic}$	Magnitude of t_{QSK} change (additive to t_{QSK_static}) under noisy conditions	Across the supported voltage-temperature range and with SSO conditions and pattern dependence included	0	0.085	0	0.085	t_{CK}	7,9,10
t_{Q2Q}	Earliest Qn Output to Latest Qn Output Skew Tolerance within the same A or B group (in the same unit)	Measured with quiet conditions, only two output switching, and nominal V-T conditions of V_{DD}=1.1V and 25℃	0	0.15	0	0.15	t_{CK}	7,9,11
t_{Qerr}	Total magnitude of t_{QSK} error $t_{Qerr} = 2x\ t_{QSK\_dynamic} + t_{Q2Q}$	Across the supported voltage-temperature range and with SSO conditions and pattern dependence included	0	0.25	0	0.25	t_{CK}	7,10
t_{ALERT}	ALERT_n propagation delay	DERROR_IN_n LOW to ALERT_n LOW	-	2	-	2	ns	12
t_{ALERT_HL}	ALERT_n assertion delay from DCK_t/DCK_c	DCK_t/DCK_c to ALERT_n LOW	-	1.5	-	1.5	ns	13
t_{RST}	RESET propagation delay	DRST_n LOW to QRST_n LOW	-	20	-	20	ns	

Symbol	Parameter	Conditions	DDR5-4400		DDR5-4800		Unit	Note
			Min	Max	Min	Max		
t_{QDIS}	Output buffers(except for QxCK_t/ QxCK_c, QxCSn) hi-z after QCS[1:0]_n goes LOW follwing SRE command	QCS[1:0]_n=LOW;DRST_n=HIGH ; DCK_t/DCK_c=toggling	2	-	2	-	t_{CK}	
$t_{SRX2QCK}$	Number of cycles from NOP command to release QCS to QCK clocks running and QCS driven HIGH	DRST_n=HIGH;DCK_t/ DCK_c=Toggling	-	16 + t_{PDM}	-	16 + t_{PDM}	t_{CK}	
t_{CASRX}	QCA HIGH to QCS HIGH when exiting SelfRefresh		0	-	0	-	ns	
t_{ODU}	Output Delay Update time	OP7=1 for RW12 to RW1E	-	100	-	100	ns	14

NOTE :

1) See diagram (Figure 120, " Test Load," on JESD82-511)
2) See diagram (Figure 7, "One UI DRAM Command Timing Diagram" on JESD82-511). t_{PDM} is defined for 0 nCK command latency adder (RW11[2:0]='000'), default (Moderate) output slew rate control settings in RW0E and RW0F, and output delay features are all enabled in RW12-RW1A but set to zero delay
3) t_{PDM} for SDR mode is measured from DCK_t/DCK_c rising edge cross point to output
4) Applies to External Loopback Only (RW26[2:0]='011' or '100')
5) Applies to Internal Loopback Only (RW26[2:0]='001' or '010')
6) This skew represents the absolute Qn skew compared to the output clock QxCK and contains the register pad skew, clock skew, package routing skew and SSO noise (See Figure 10, "Qn Output Skew," on page 41(JESD82-511)). The output clock jitter is not included in this skew. The measurement is averaged. The Qn output can be either early or late relative to the output clocks in the channel. For outputs QxCA[13:0]_N, QxCS[1:0]_N_n, this parameter applies to each of the two A/B output groups independently per channel. This parameter also applies to the BCOM[2:0]_N and BCS_N_n outputs w.r.t. to the output clock BCK_N
7) The values for this parameter are defined for default settings in the output delay control words RW12 to RW1E and default settings in the driver char-acteristics and slew rate control words RW0A through RW0F
8) This skew represents the absolute Qn skew compared to the output clock QxCK and contains the register pad skew, clock skew, and package routing skew at nominal V-T conditions of VDD = 1.1 V and 25°C (See Figure 10, "Qn Output Skew," on JESD82-511). The output clock jitter is not included in this skew. The measurement is averaged. The Qn output can be either early or late relative to the output clocks in the channel. For outputs QxCA[13:0]_N, QxCS[1:0]_N_n, this parameter applies to each of the two A/B output groups independently per channel. This parameter also applies to the BCOM[2:0]_N and BCS_N_n outputs w.r.t. to the output clock BCK_N. In this test, a single output signal switches with clock-like pattern of repeating 6"1s" and 6 "0s" while all other outputs remaining stable (HIGH)
9) tQSK_dynamic represents the largest change in output skew (relative to tQSK_static) within an output signal group in either direction (i.e., Early signals moving to an earlier time or Late signals moving to a later time). The output clock jitter is not included in this skew. The measurement is averaged. In this test, all outputs send patterns simultaneously to excite realistic on-die noise and crosstalk
10) tQerr imposes an additional constraint on the maximum value for the total of 2 x tQSK_dynamic + tQ2Q measured per individual unit. The device shall meet tQerr(max) in addition to meeting tQSK_dynamic(max) and tQ2Q(max)
11) This parameter represents the absolute Qn skew between earliest and latest signals within the same A/B group and contains the register pad skew and package routing skew (See Figure 10, "Qn Output Skew," on JESD82-511). The measurement is averaged.. For outputs QxCA[13:0]_N, this parameter ap-plies to each of the two A/B output groups independently per channel. Similarly, for outputs QxCS[1:0]_N_n, this parameter applies to each of the two A/B output groups independently per channel. This parameter also applies to the {BCOM[2:0]_N, BCS_N_n} output groups independently per channel.In this test, a single output signal switches with clock-like pattern of repeating 6 "1s" and 6 "0s" while all other outputs remaining stable (HIGH)
12) See Figure 117, "Voltage waveforms, tALERT Measurement," on JESD82-511
13) See Figure 120, "Test Load," on JESD82-511 and .Figure 118, "Voltage waveforms, tALERT_HL Measurement," on JESD82-511
14) This is the time the RCD requires to update delay timing setting to the output after it receives RW write

7.3 Output Clock Driver Characteristics

[Table 10] Output Clock Driver Characteristics

Symbol	Parameter	Conditions	DDR5-4400		DDR5-4800		Unit	Note
			Min	Max	Min	Max		
t_{STAB01}	RCD Stabilization time from start of DCK toggle to PLL lock	DCK_t/DCK_c stable	-	3.5	-	3.5	us	
t_{STAB02}	RCD Stabilization time from control word write to PLL lock	DCK_t/DCK_c stable	-	25.0	-	25.0	us	1
t_{STAB_DB}	Data Buffer Stabilization time	BCK_t/BCK_c stable	See DDR5DB01 Specification		See DDR5DB01 Specification		us	
t_{STAB_DBCMD}	LRDIMM stabilization time for commands not requiring use of data path	DCK_t/DCK_c stable	-	3.5	-	3.5	us	2,3
t_{STAB_DBDATA}	LRDIMM stabilization time for commands requiring use of data path	DCK_t/DCK_c stable	-	4.14	-	4.14	us	3,4
t_{CKsk}	Fractional Clock Output Skew		-	20	-	20	ps	5
t_{staoff}	Clock delay through the register between the input clock and output clock		Min:(tPDM(min) + 1/2 tCK); Max: (tPDM(max) + 1/2 tCK)		Min:(tPDM(min) + 1/2 tCK); Max: (tPDM(max) + 1/2 tCK)		ps	6,7
t_{dynoff}	Maximum re-driven dynamic clock offset		-	35	-	35	ps	8,9

NOTE :

1) This parameter applies to control word writes to RW05/RW06 and Bit OP0 in RW00
2) Measured from start of DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface but does not require the use of data path (e.g., SRX, NOP, etc.)
3) Applies only to Self Refresh Exit without frequency change.
4) Measured from start of DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface and requires the use of data path (e.g., WR, RD)
5) This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 101 on JESD82-511). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to right side clock pairs between QACK_A_t/QACK_A_c and QCCK_A_t/QCCK_A_c, as well as left side of the clock pairs between QA-CK_B_t/QACK_B_c and QCCK_B_t/QCCK_B_c. Similarly, to right side clock pairs between QBCK_A_t/QBCK_A_c and QDCK_A_t/QDCK_A_c, as well as left side of the clock pairs between QBCK_B_t/QBCK_B_c and QDCK_B_t/QDCK_B_c.This is not a tested parameter and has to be considered as a design goal only
6) RW05/RW06 must be set to correct speed and the device must run at one of the speed nodes defined in Table 190 on JESD82-511. See Figure 99 and Figure JESD82-511
7) This measures the delay from the rising differential input clock which samples incoming DCA to the rising differential output clock that will be used to sample the same QCA data. The parameter describes the maximum and minimum QxCK clock tPD.
8) VDD measurement DC bandwidth is limited to 20 MHz
9) See Figure 99 and Figure 100 on JESD82-511

7.4 Output Clock Jitter Parameters

[Table 11] Tx QCK Jitter Specifications

[BUJ = Bounded Uncorrelated Jitter; DCD = Duty Cycle Distortion; Dj = Deterministic Jitter; Rj = Random Jitter; pp = Peak-to-Peak]

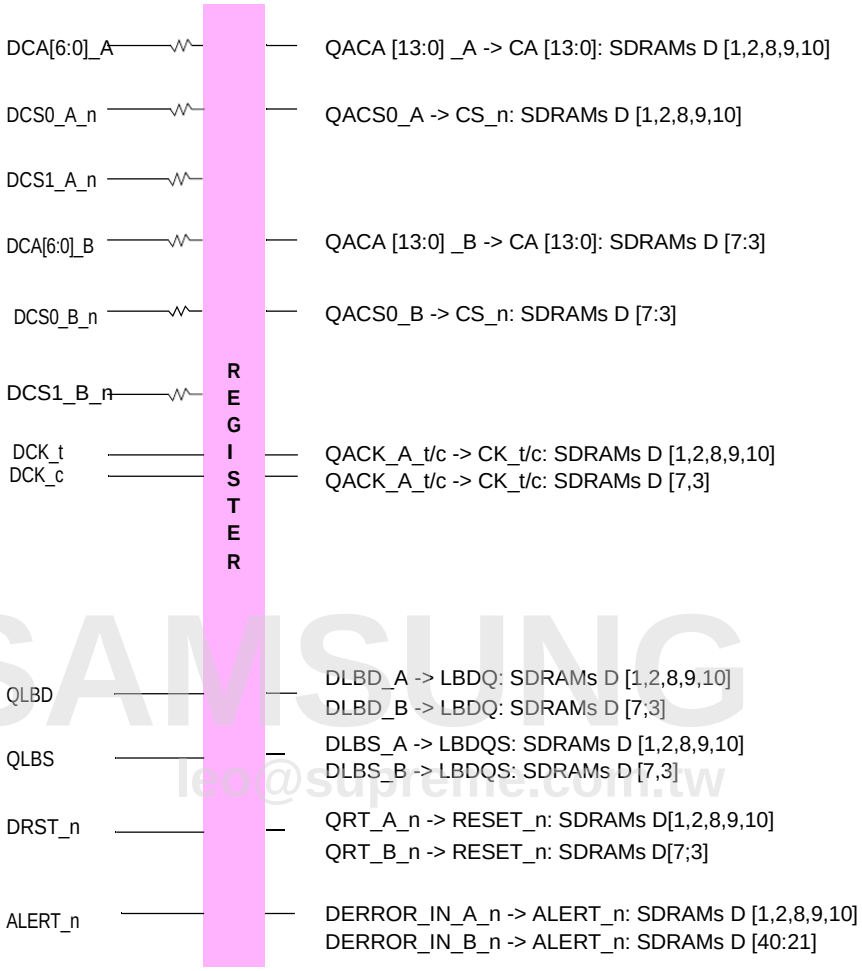
Symbol	Parameter	DDR5-4400		DDR5-4800		Unit	NOTE
		Min	Max	Min	Max		
tTx_QCK_1UI_Rj_NoBUJ	Rj value of 1-UI Jitter without BUJ	-	0.0035	-	0.0035	UI (RMS)	1,2,3
tTx_QCK_1UI_Dj_NoBUJ	Dj pp value of 1-UI Jitter without BUJ	-	0.09	-	0.09	UI	1,3,4
tTx_QCK_NUI_Rj_ NoBUJ, where 1 < N < 4	Rj value of N-UI Jitter without BUJ, where 1 < N < 4	-	0.0035	-	0.0035	UI (RMS)	1,3,5
tTx_QCK_NUI_Dj_ NoBUJ, where 1 < N < 4	Dj pp value of N-UI Jitter without BUJ, where 1 < N < 4	-	0.09	-	0.09	UI	1,3,6
tTx_QCK_NUI_Rj_ NoBUJ, where 3 < N < 31	Rj value of N-UI Jitter without BUJ, where 3 < N < 31	-	TBD	-	TBD	UI (RMS)	1,3,7
tTx_QCK_NUI_Dj_ NoBUJ, where 3 < N < 31	Dj pp value of N-UI Jitter without BUJ, where 3 < N < 31	-	TBD	-	TBD	UI	1,3,8
Unit UI = tCK(avg).min/2							

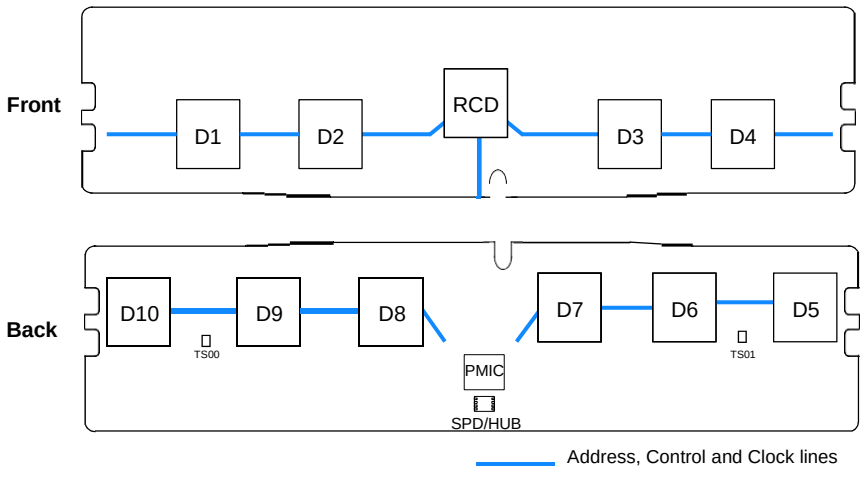
NOTE :
1) When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or cannot be esti-mated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
2) Rj RMS value of 1-UI jitter without BUJ. This extraction is to be done after software correction of DCD
3) This test should be done in typical temperature and voltage conditions (i.e., VDD = 1.1 V, 25 °C)
4) Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ. Dj indicates Djdd of dual-Dirac fitting
5) Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
6) Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after soft-ware correction of DCD
7) Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
8) Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

8.0 FUNCTION BLOCK DIAGRAM

8.1 16GB, x80 DIMM (Populated as 1rank of x8 DDR5 SDRAMs)

8.1.1 16GB, x80 DIMM (Populated as 1rank of x8 DDR5 SDRAMs) - Part 1 of 4



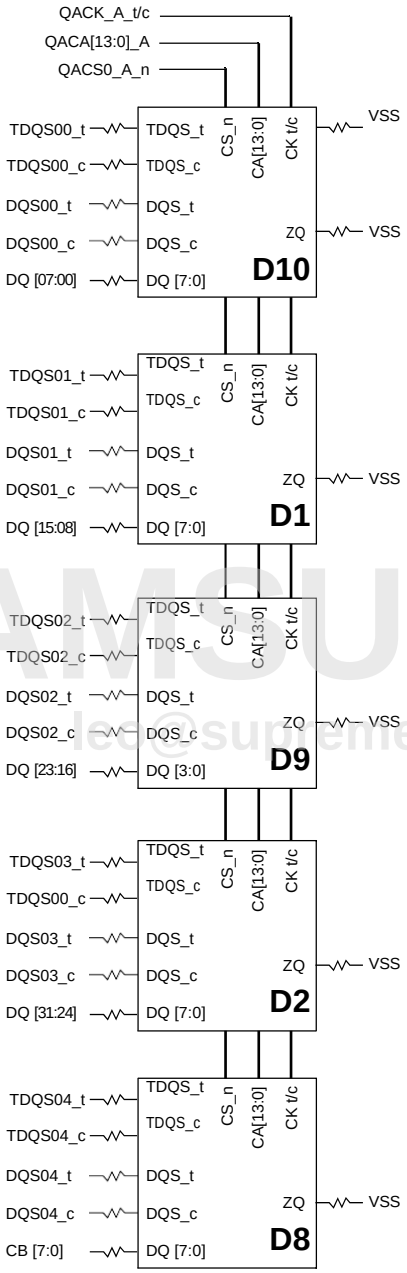


NOTE :

1) Unless otherwise noted resistors are 15Ω ± 5%

8.1.2 16GB, x80 DIMM (Populated as 1rank of x8 DDR5 SDRAMs) - Part 2 of 4

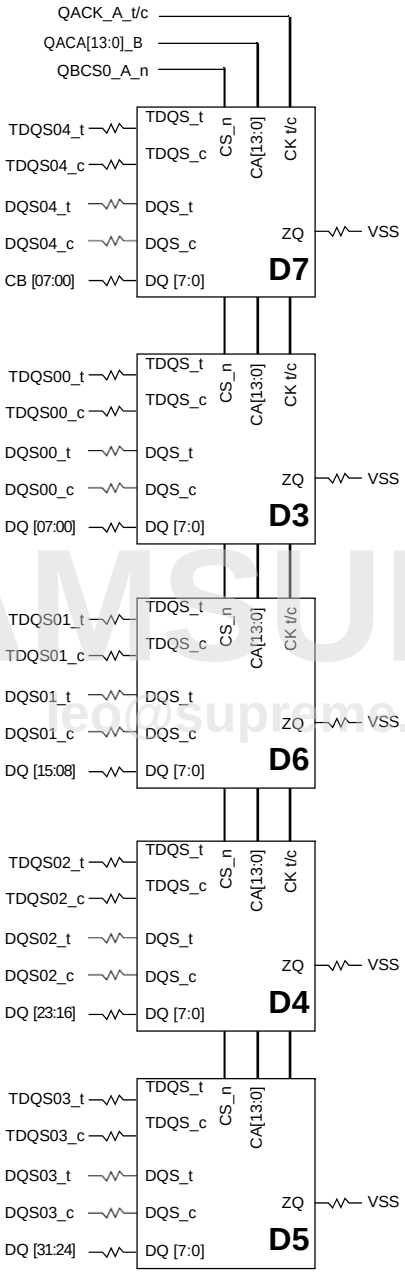
Channel A



NOTE :
1) Unless otherwise noted resistors are 15Ω ± 5%
2) ZQ resistors are 240Ω ± 1%

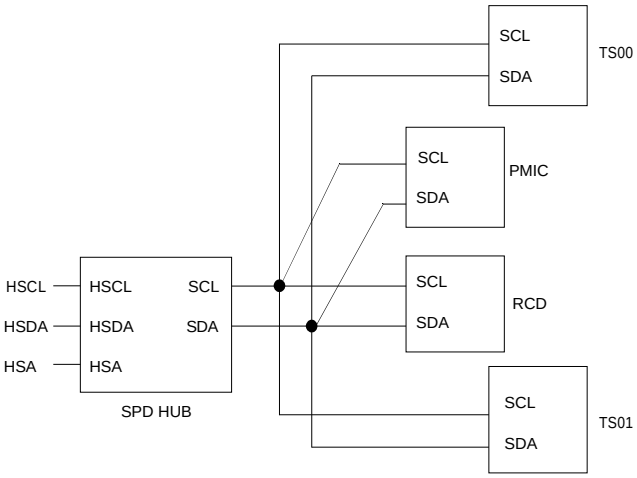
8.1.3 16GB, x80 DIMM (Populated as 1rank of x8 DDR5 SDRAMs) - Part 3 of 4

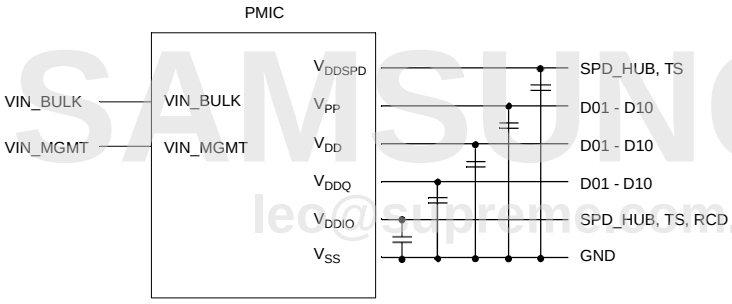
Channel B



NOTE :
1) Unless otherwise noted resistors are 15Ω ± 5%
2) ZQ resistors are 240Ω ± 1%

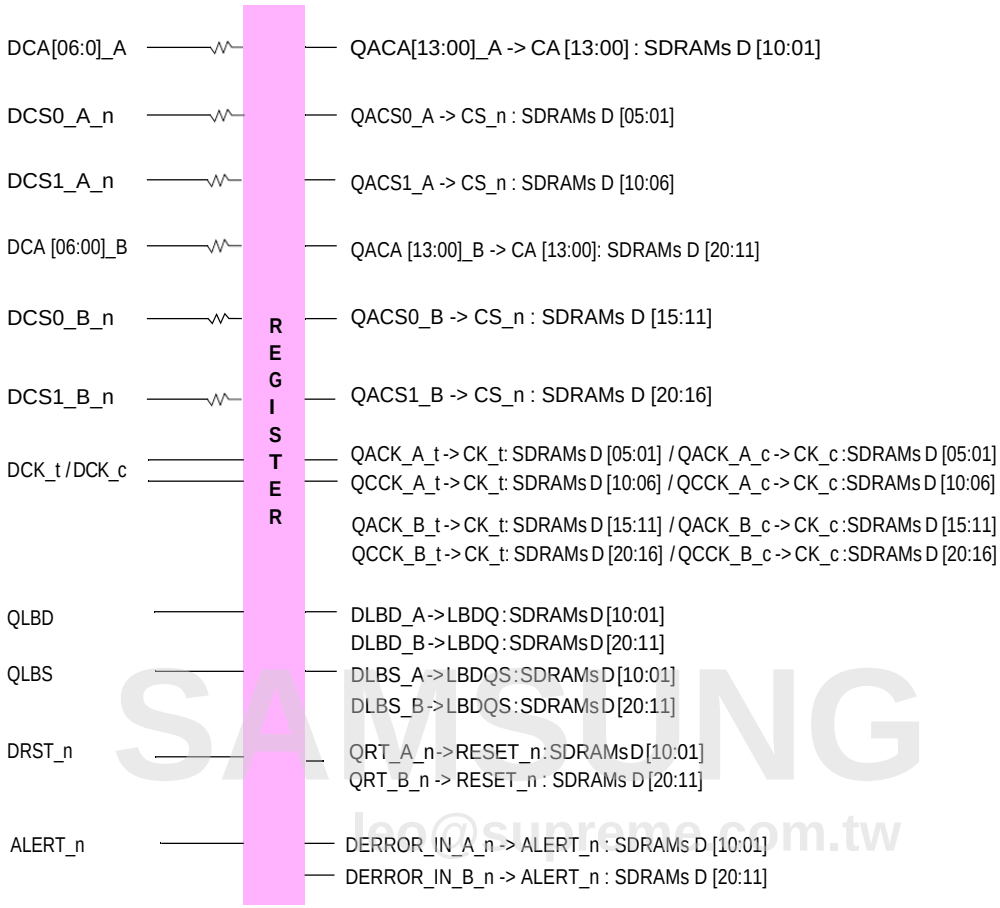
8.1.4 16GB, x80 DIMM (Populated as 1rank of x8 DDR5 SDRAMs) - Part 4 of 4

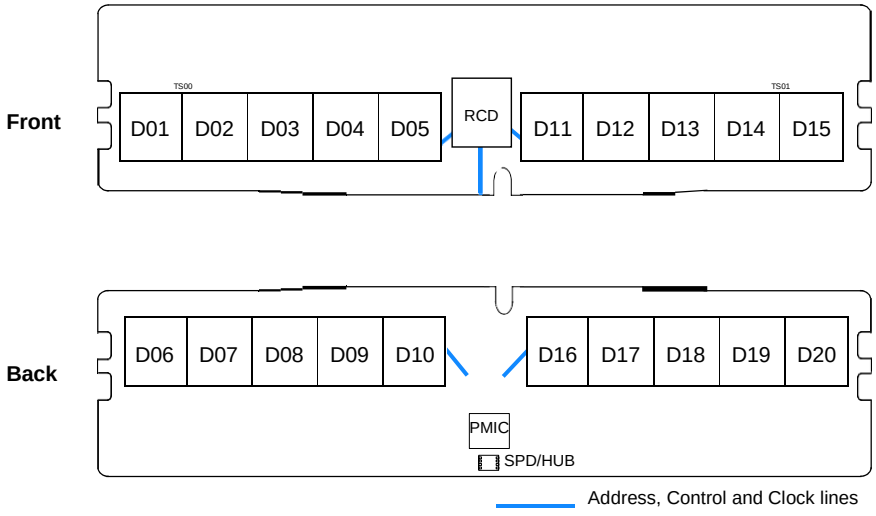




8.2 32GB, x80 DIMM (Populated as 2 ranks of x8 DDR5 SDRAMs)

8.2.1 32GB, x80 DIMM (Populated as 2 ranks of x8 DDR5 SDRAMs) - Part 1 of 4

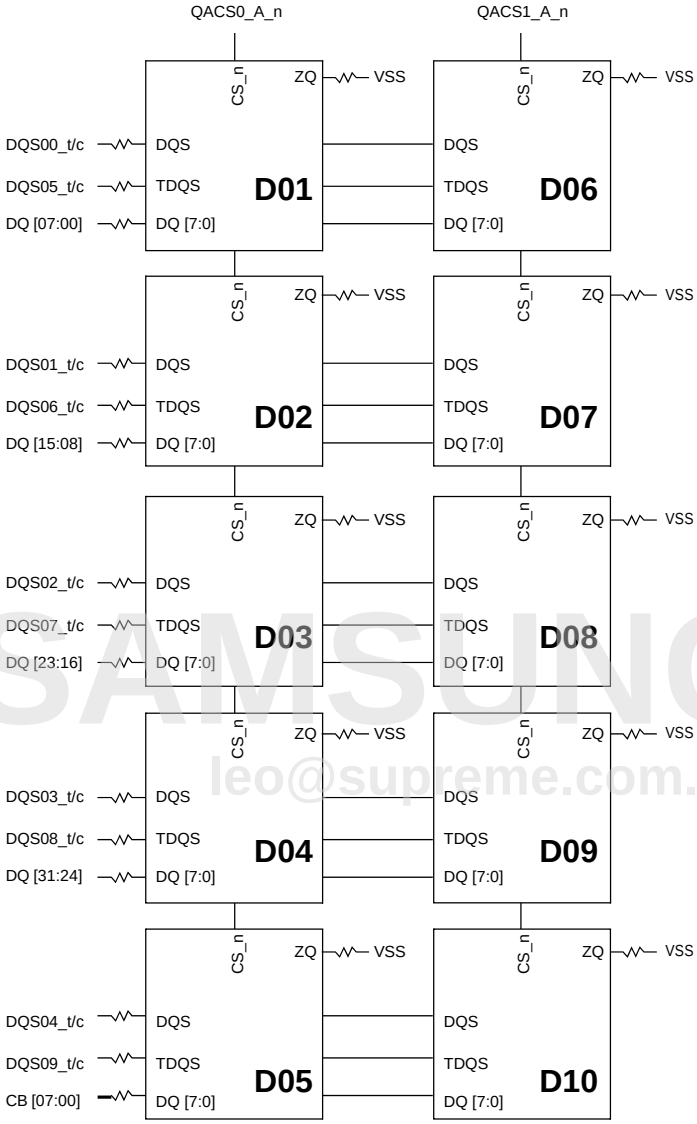




NOTE :
1) Unless otherwise noted resistors are 15Ω ± 5%

8.2.2 32GB, x80 DIMM (Populated as 2 ranks of x8 DDR5 SDRAMs) - Part 2 of 4

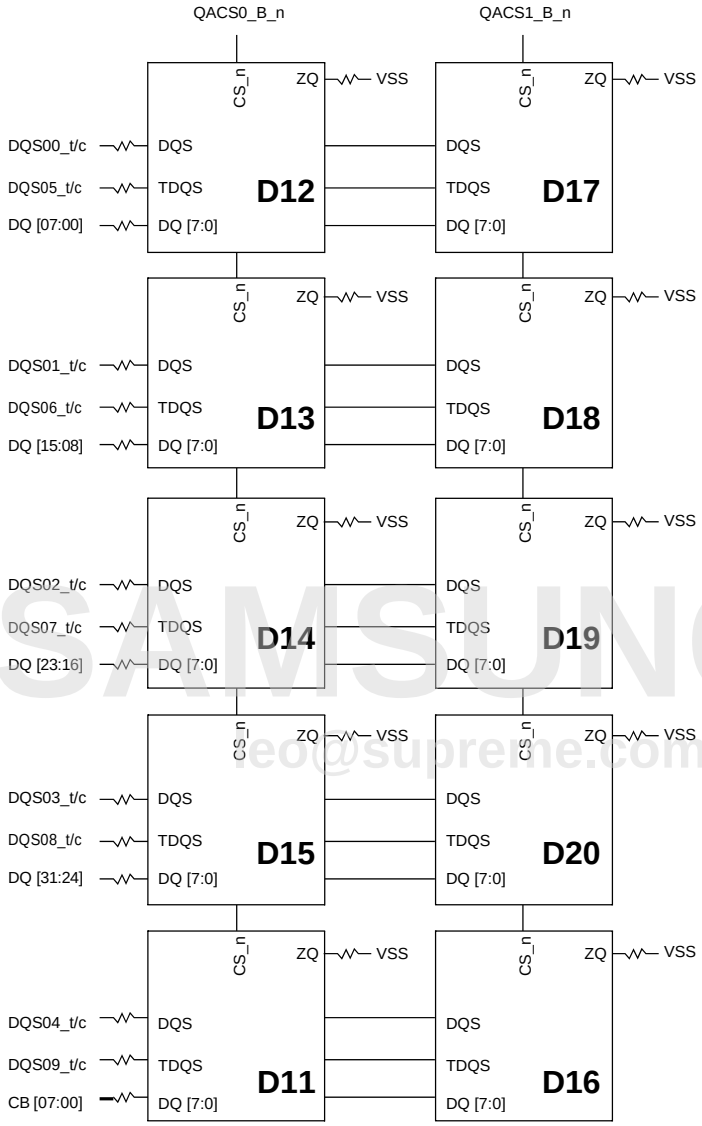
Channel A



NOTE:
1) Unless otherwise noted resistors are 15Ω ± 5%
2) ZQ resistors are 240Ω ± 1%

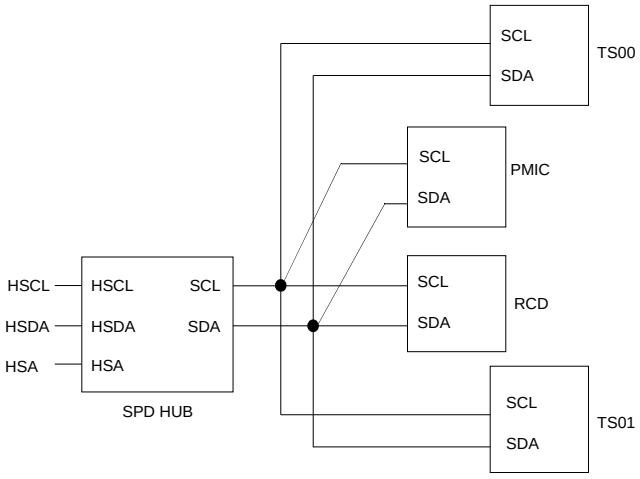
8.2.3 32GB, x80 DIMM (Populated as 2 ranks of x8 DDR5 SDRAMs) - Part 3 of 4

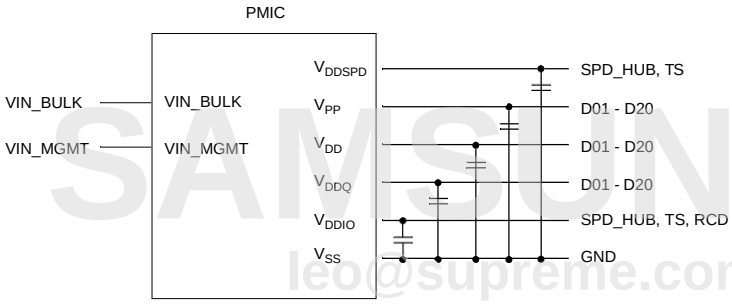
Channel B



NOTE :
1) Unless otherwise noted resistors are 15Ω ± 5%
2) ZQ resistors are 240Ω ± 1%

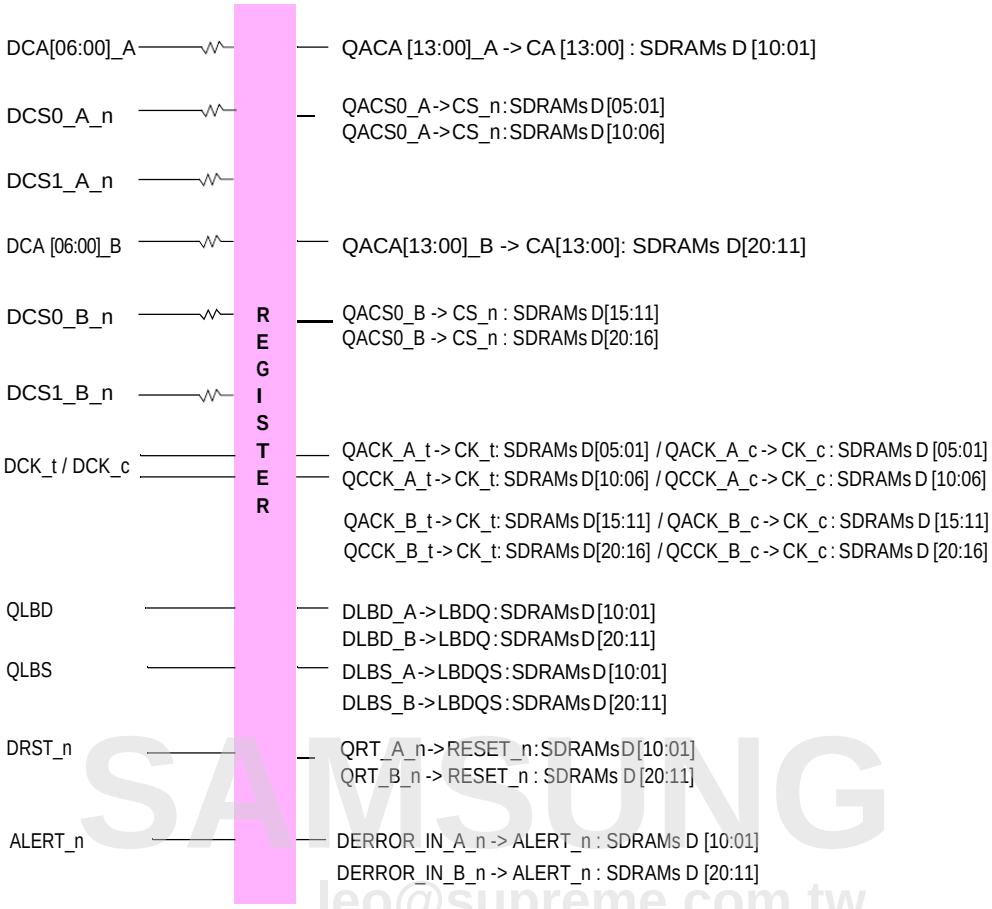
8.2.4 32GB, x80 DIMM (Populated as 2 ranks of x8 DDR5 SDRAMs) - Part 4 of 4

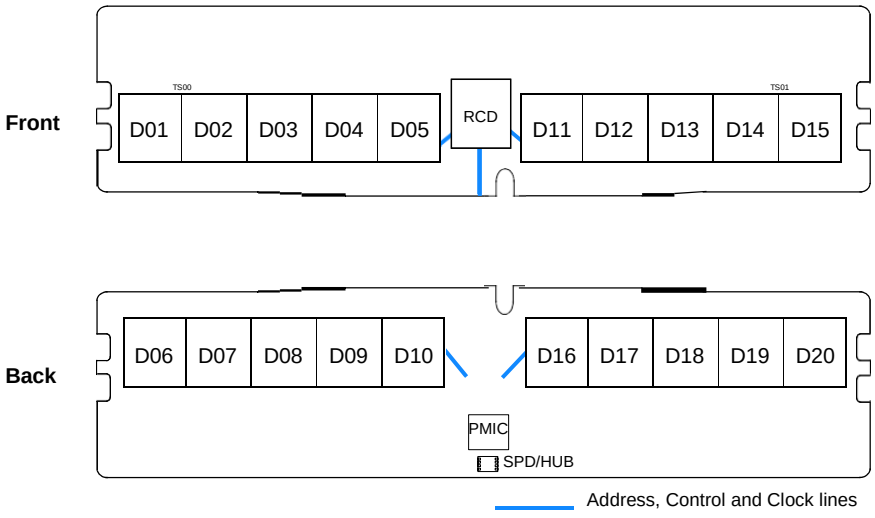




8.3 32GB, x80 DIMM (Populated as 1 rank of x4 DDR5 SDRAMs)

8.3.1 32GB, x80 DIMM (Populated as 1 rank of x4 DDR5 SDRAMs) - Part 1 of 4

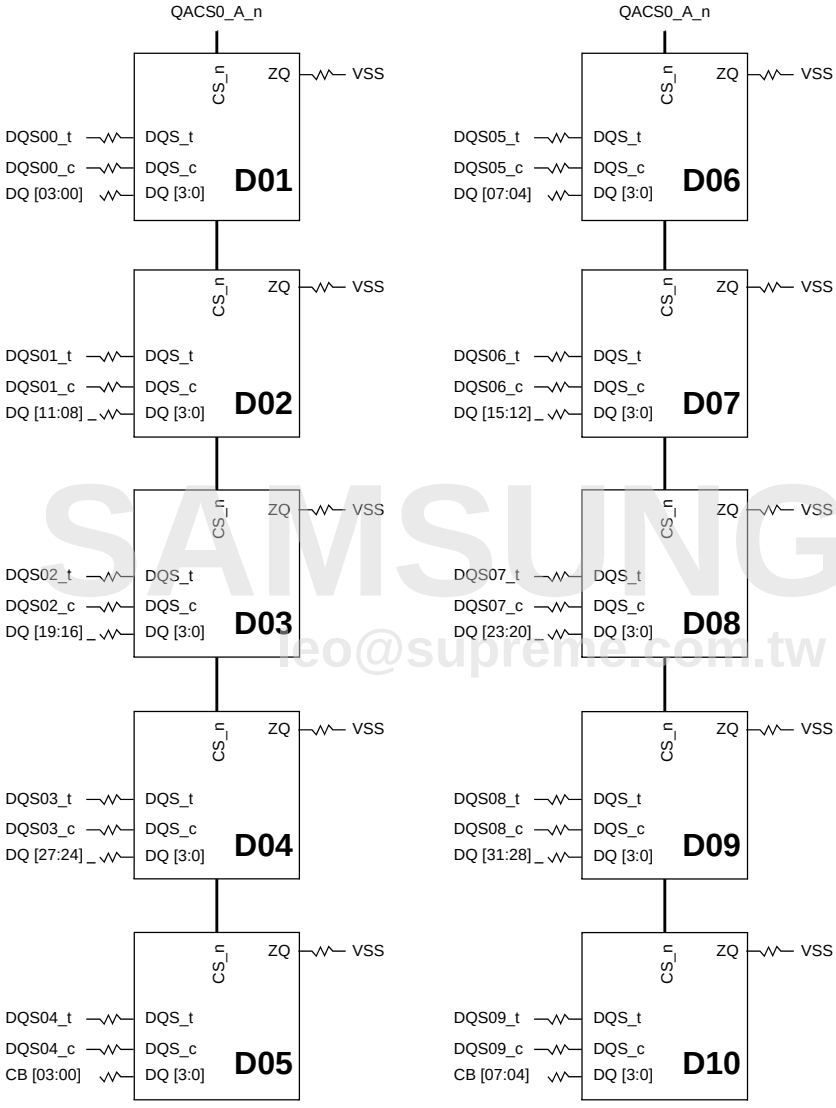




NOTE :
1) Unless otherwise noted resistors are 15Ω ± 5%

8.3.2 32GB, x80 DIMM (Populated as 1 rank of x4 DDR5 SDRAMs) - Part 2 of 4

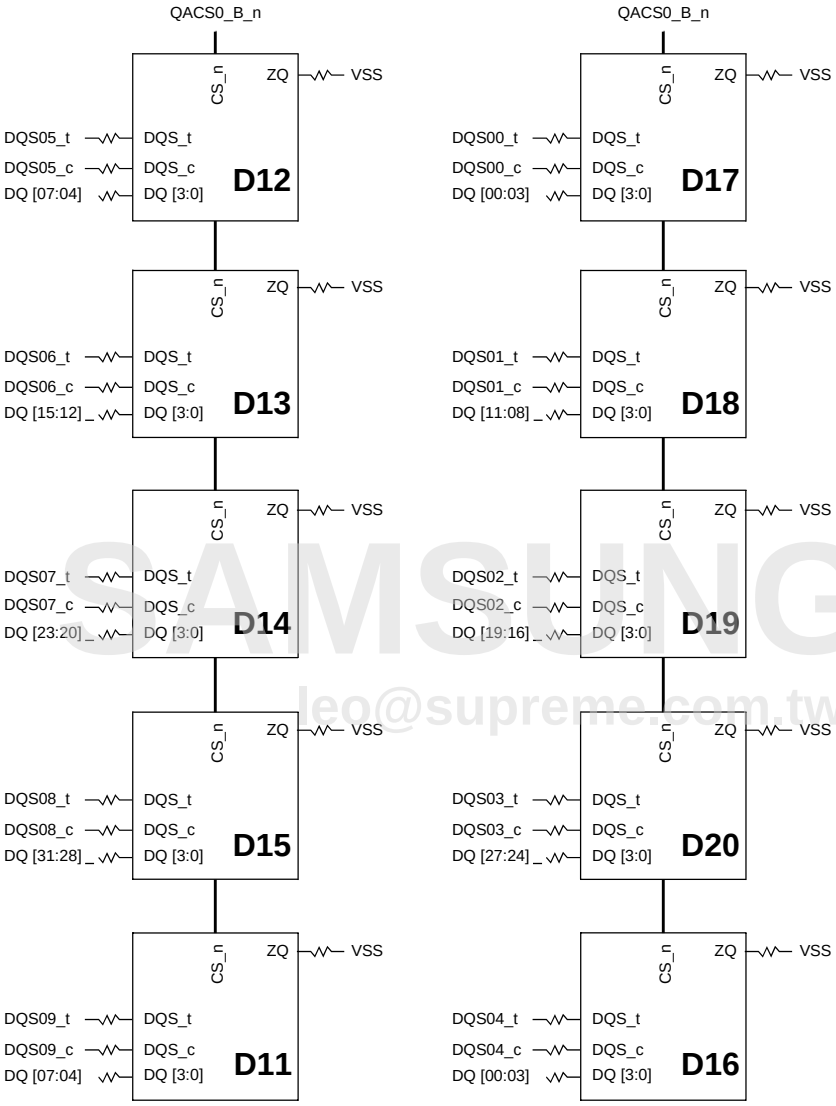
Channel A



NOTE:
1) Unless otherwise noted resistors are 15Ω ± 5%
2) ZQ resistors are 240Ω ± 1%

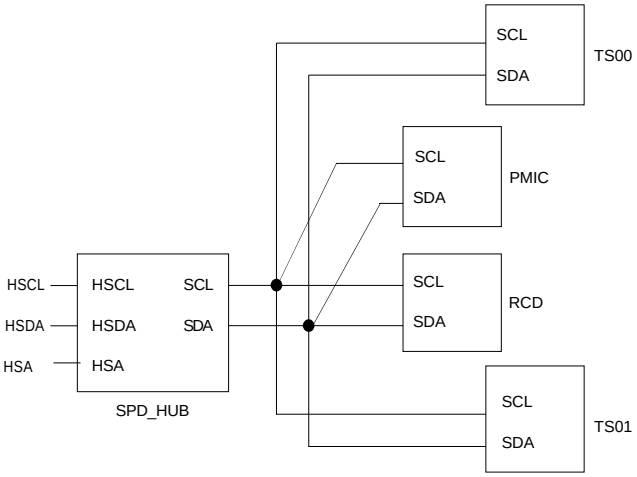
8.3.3 32GB, x80 DIMM (Populated as 1 rank of x4 DDR5 SDRAMs) - Part 3 of 4

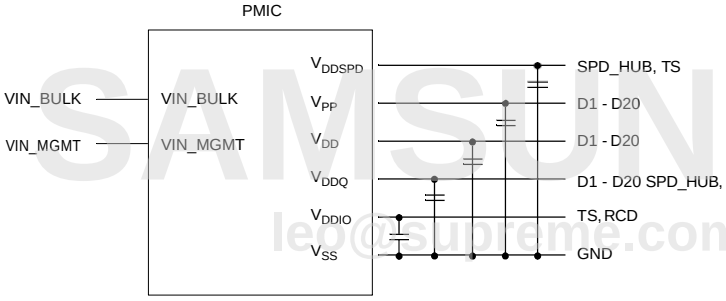
Channel B



NOTE:
1) Unless otherwise noted resistors are 15Ω ± 5%
2) ZQ resistors are 240Ω ± 1%

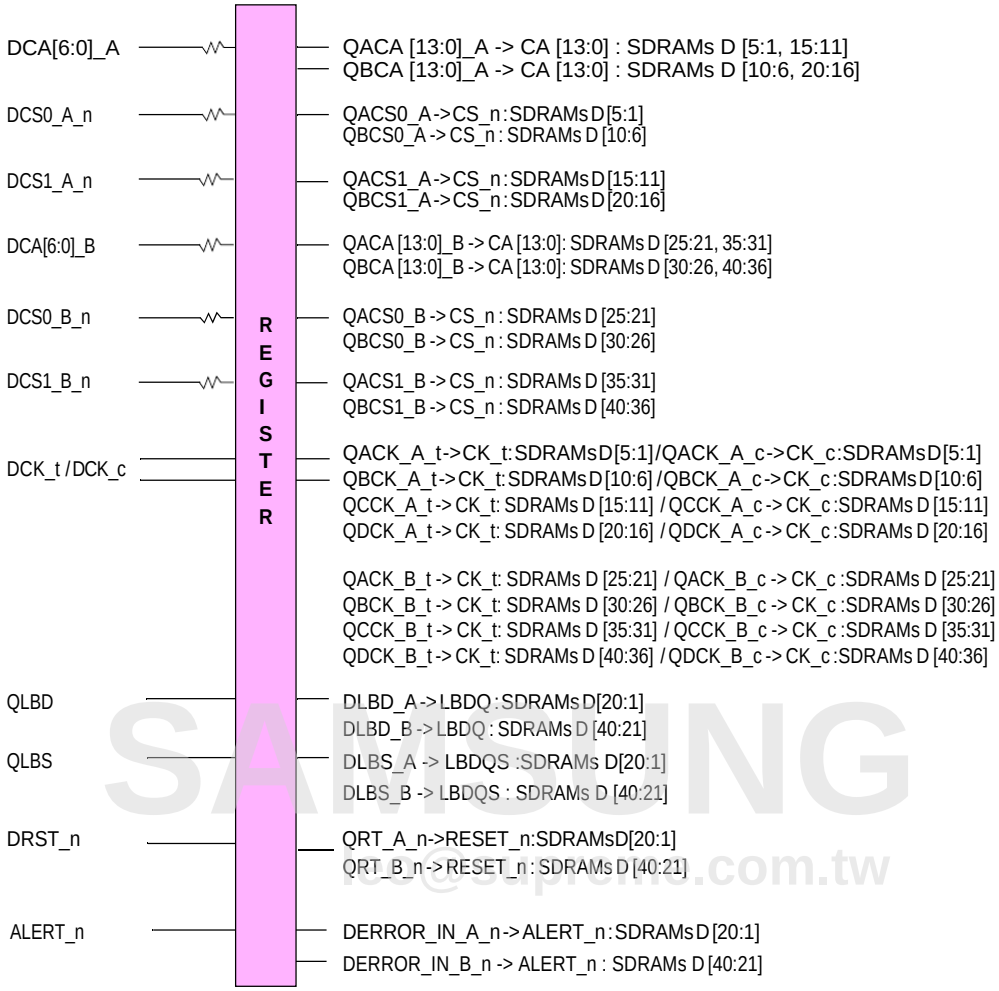
8.3.4 32GB, x80 DIMM (Populated as 1 rank of x4 DDR5 SDRAMs) - Part 4 of 4

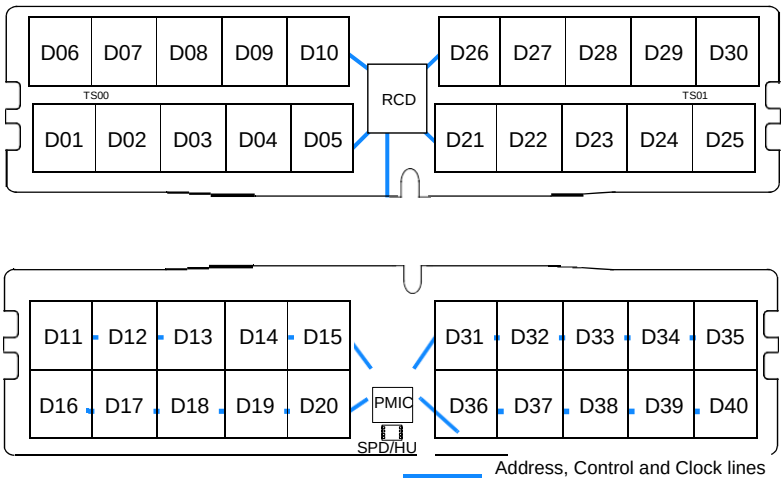




8.4 64GB,x80 DIMM(Populated as 2 ranks of x4 DDR5 SDRAMs)

8.4.1 64GB,x80 DIMM(Populated as 2 ranks of x4 DDR5 SDRAMs) - Part 1 of 4

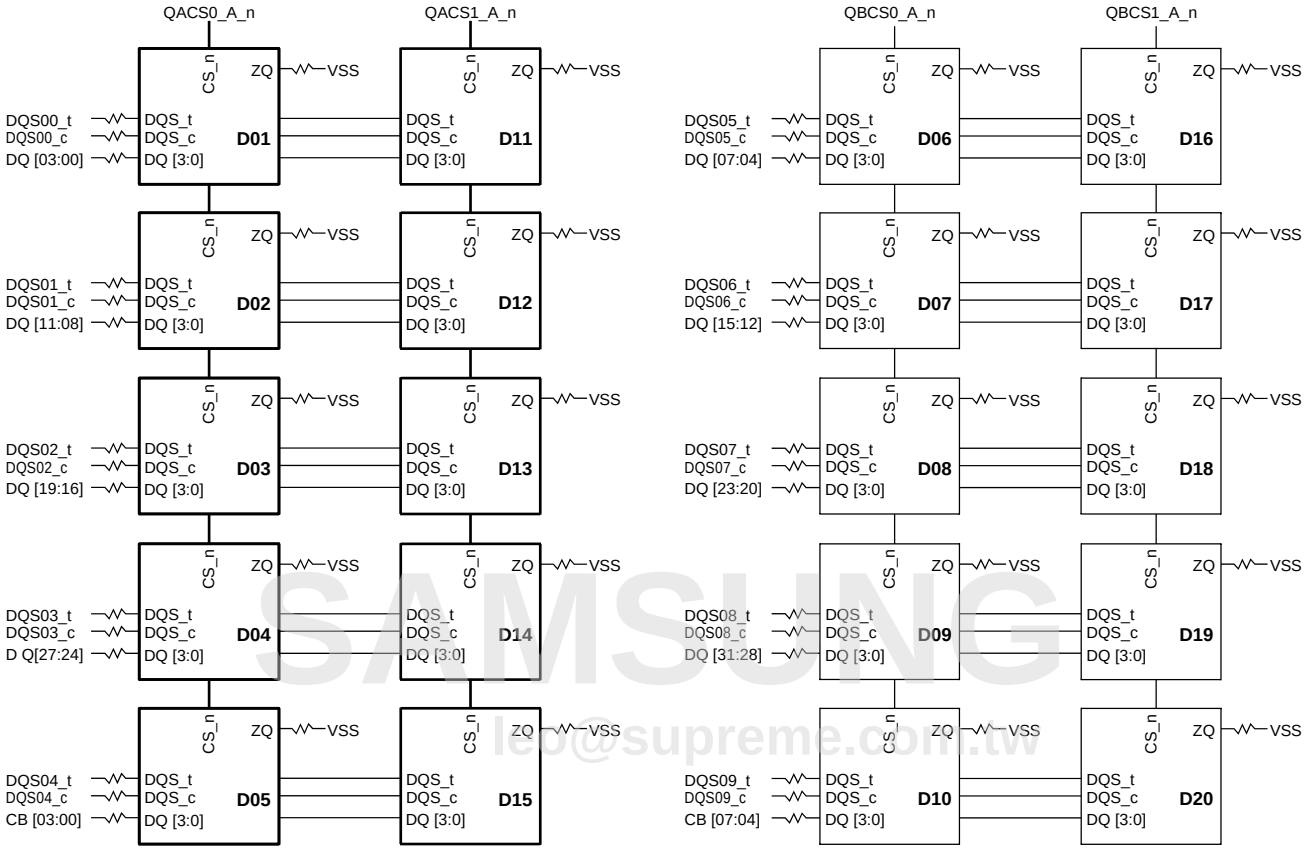




NOTE :
1) Unless otherwise noted resistors are 15Ω ± 5%

8.4.2 64GB,x80 DIMM (Populated as 2 ranks of x4 DDR5 SDRAMs) - Part 2 of 4

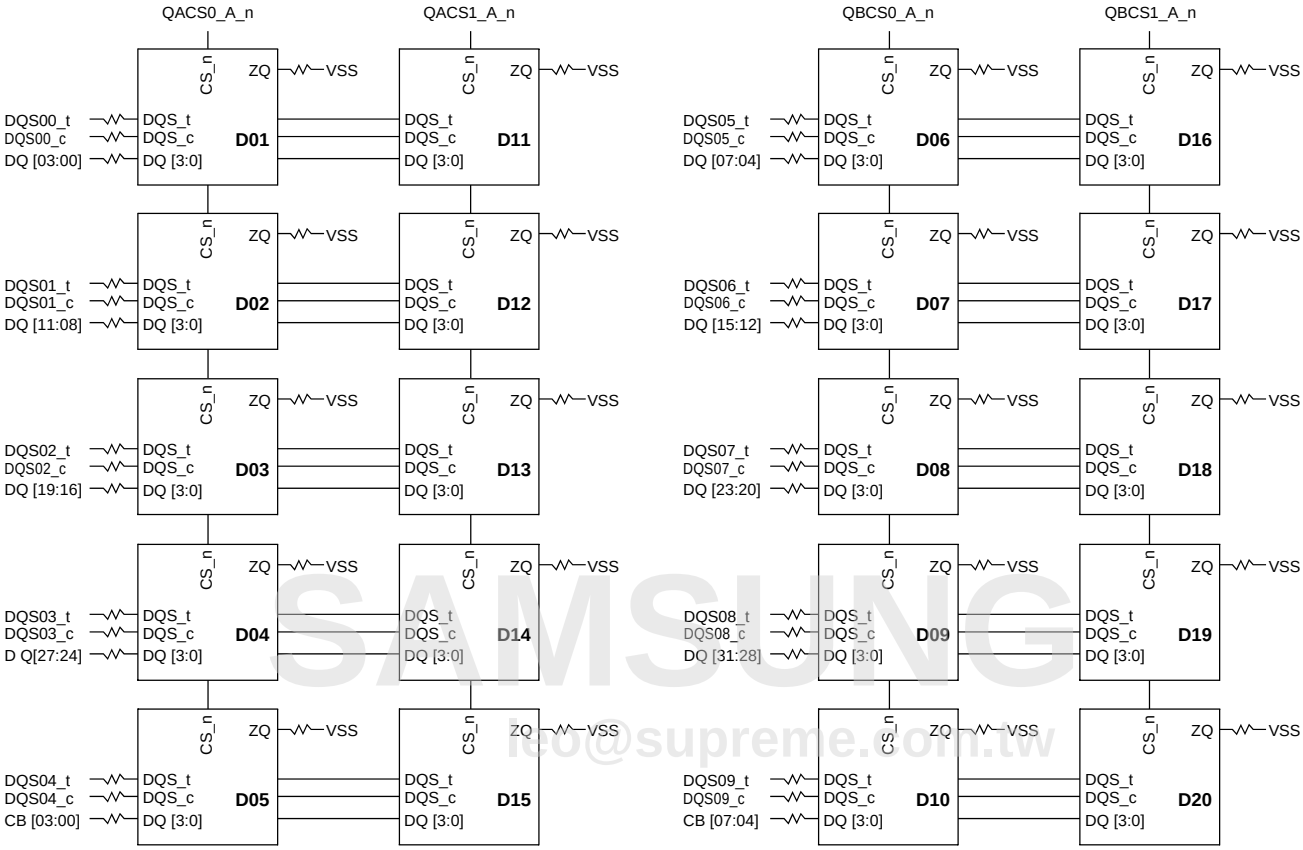
Channel A



NOTE :
1) Unless otherwise noted resistors are 15Ω ± 5%
2) ZQ resistors are 240Ω ± 1%

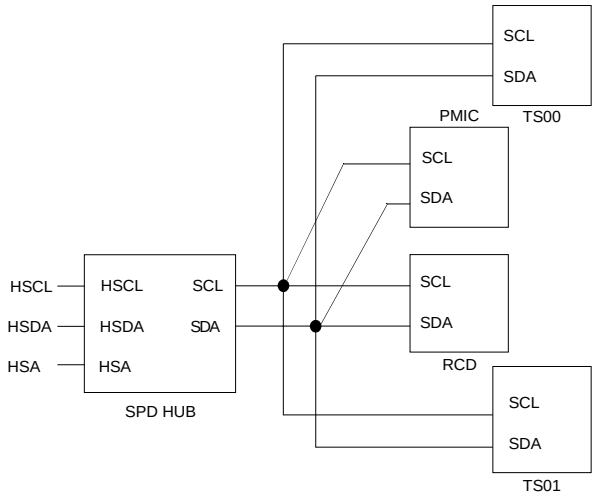
8.4.3 64GB,x80 DIMM (Populated as 2 ranks of x4 DDR5 SDRAMs) - Part 3 of 4

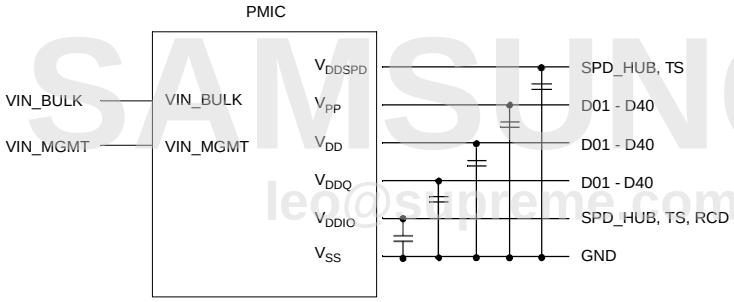
Channel B



NOTE :
1) Unless otherwise noted resistors are 15Ω ± 5%
2) ZQ resistors are 240Ω ± 1%

8.4.4 64GB,x80 DIMM (Populated as 2 ranks of x4 DDR5 SDRAMs) - Part 4 of 4





9.0 AC & DC OPERATING CONDITIONS

9.1 DIMM Voltage Requirements

The DIMM input voltage requirements and the SDRAM voltage requirements are not identical. The DIMM voltage requirements must meet the PMIC input voltage requirements. The PMIC output voltage requirements must meet the voltage requirements of SDRAM, RCD, Data Buffer, Hub and Temperature Sensors. There must be some allowance for a small voltage drop across the DIMM for both supply voltages and PMIC output voltages. Table 12 defines the requirements from the Host at the DIMM socket to the PMIC inputs, and the PMIC outputs.
Some DIMMs have lower current requirements. Each specific DIMM configuration must meet the voltage requirements for its worst-case load currents.

[Table 12] DDR5 RDIMM DC Operating Voltage

Symbol	Parameter	Voltage Rating (Volts)			Maximum Expected Current (Amps)	Power State
		Minimum	Typical	Maximum		
VIN_BULK	Host Supply Voltage	4.25	12.0	15	2.5(maximum)	Operational
VIN_MGMT	Host Supply Voltage	3.0	3.3	3.6	0.110(minimum)	Operational
VDD	PMIC Output Supply Voltage	1.067	1.1	1.166	Note 5	Operational
VDDQ	PMIC Output Supply Voltage	1.067	1.1	1.166	Note 5	Operational
VPP	PMIC Output Supply Voltage	1.746	1.8	1.908	Note 5	Operational
1.8V LDO	PMIC Output Supply Voltage	Note 6	1.8	Note 6	0.025(maximum)	Operational
1.0V LDO	PMIC Output Supply Voltage	Note 6	1.0	Note 6	0.020(maximum)	Operational

NOTE :
1) The SDRAM specification must be met and takes precedence over this document.
2) PMIC, Hub, TS, RCD specifications must be met and takes precedence over this document.
3) Maximum current establishes the platform maximum current regulation point. It provides a data point for DIMM developers to set power plane impedances.
4) Typical voltage is platform dependent. This is a suggested value only.
5) Maximum and Minimum Current ratings depend on PMIC (5000 or 5010), and number of DRAM and Data Buffers placed.
6) See PMIC supplier datasheet for Minimum and Maximum ratings.

9.2 Recommended Operating Temperature Ranges

[Table 13] Recommended Operating Temperature Ranges

Parameter/Condition	Device Rating	Symbol	Min	Normal	Extended
Commercial Temperature	CT	TOPER-CT	0ºC	85ºC	95ºC
Industrial Temperature	IT	TOPER-IT	-40ºC	85ºC	95ºC

NOTE :
1) The operating temperature is the case surface temperature on the center-top side of the DDR5 device. For measurements conditions, refer toJESD51-2
2) Normal is the maximum limit when device is operating in the Normal Temperature Mode
3) Extended is the maximum limit when device is operating in the Extended Temperature Mode
4) Support for the Industrial Temperature device is TBD

10.0 AC & DC INPUT MEASUREMENT LEVELS

10.1 CA Rx Voltage and Timings

NOTE: The following draft assumes internal CA VREF. If the VREF is external, the specs will be modified accordingly.
The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.
The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

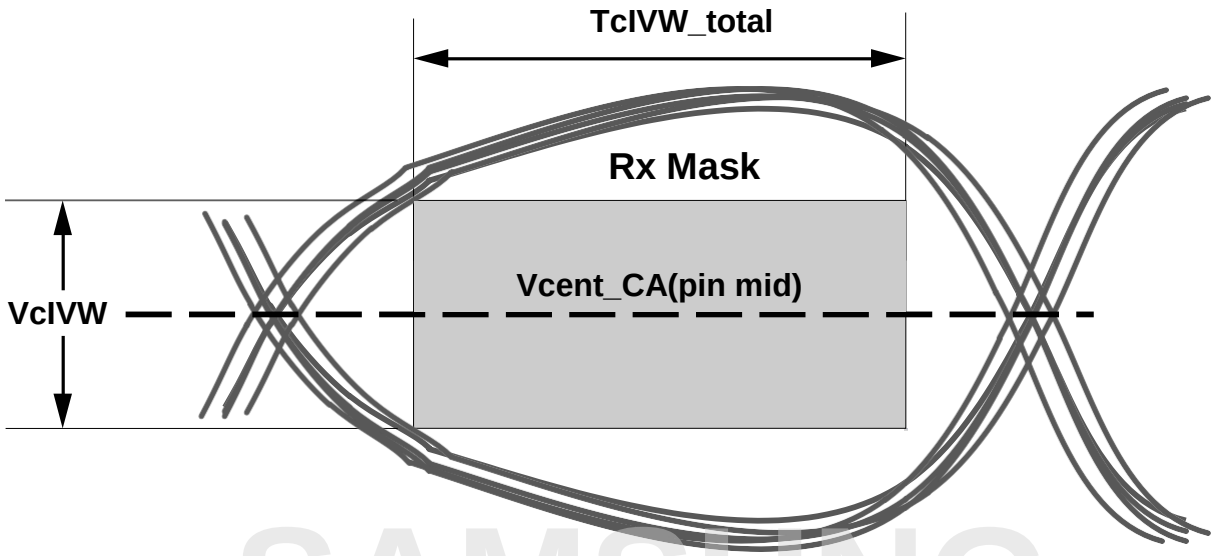


Figure 3. CA Receiver (Rx) mask

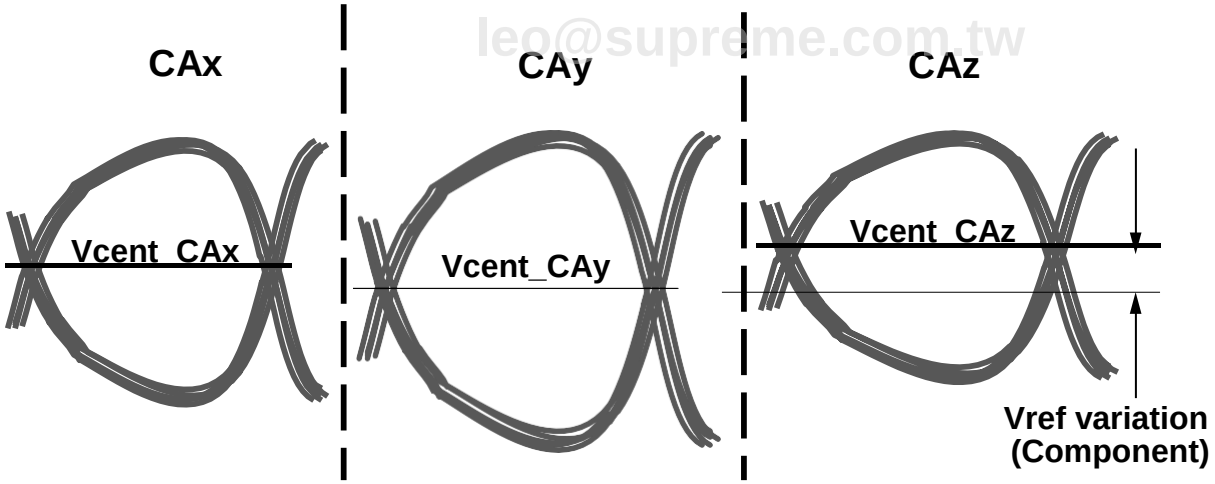


Figure 4. Across pin V_{REF}CA voltage variation

Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 5. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level VREF will be set by the system to account for Ron and ODT settings.

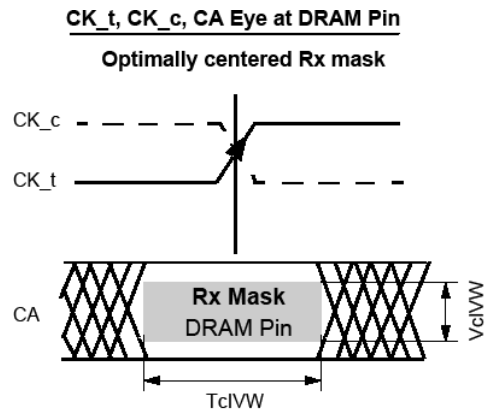
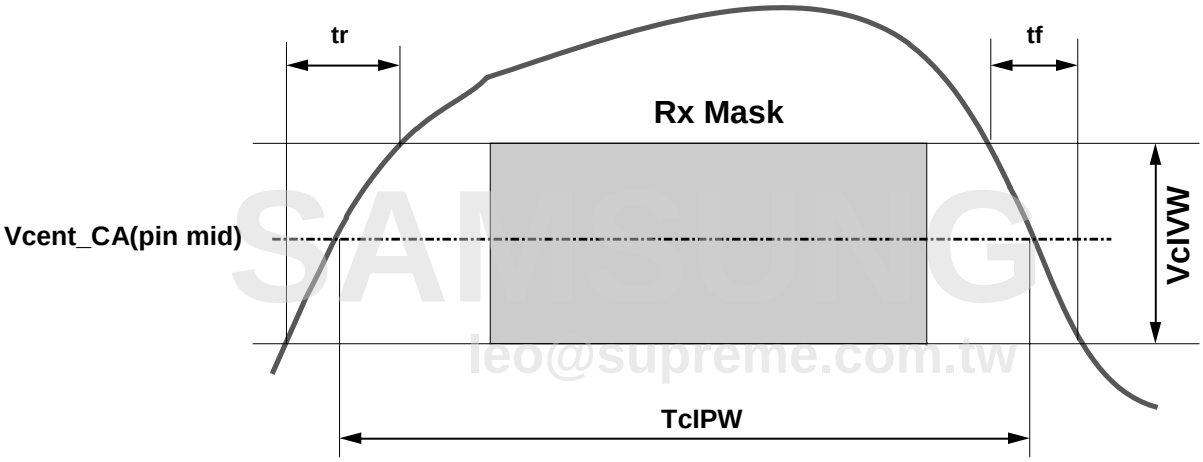


Figure 5. CA Timings at the DRAM Pins



NOTE :

1) SRIN_clVW=VclVW_Total/(tr or tf), signal must be monotonic within tr and tf range

Figure 6. CA TclPW and SRIN_clVW definition (for each input pulse)

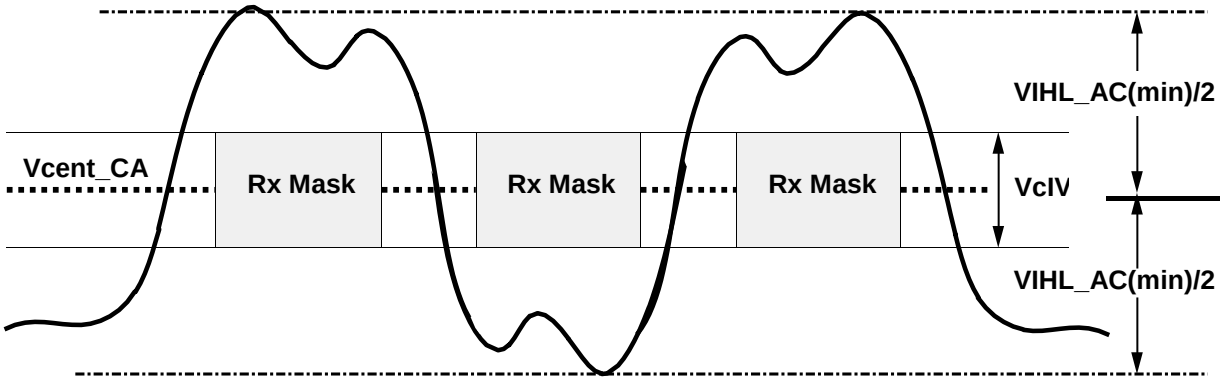


Figure 7. CA VIHL_AC definition (for each input pulse)

[Table 14] DRAM CA, CS Parametric values

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	-	130	-	130	mV	1,2,4
Rx Timing Window	TcIVW	-	0.2	-	0.2	UI*	1,2,3,4,8
CA Input Pulse Amplitude	VIHL_AC	150		150		mV	7
CA Input Pulse Width	TcIPW	0.58		0.58		UI*	5,8
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	V/ns	6

NOTE :
1) CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2) Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3) Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
4) Defined over the CA internal VREF range. The Rx mask at the pin must be within the internal VREF CA range irrespective of the input signal com-mon mode.
5) CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6) Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
7) VIHL_AC does not have to be met when no transitions are occurring.
8) * UI=tCK(avg)min.

10.2 Input Clock Jitter Specification

10.2.1 Overview

The clock is being driven to the DRAM either by the RCD for RDIMM modules. (Figure 8)

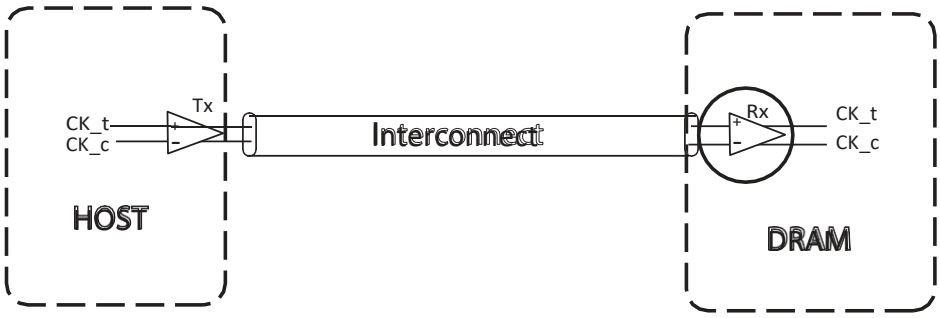


Figure 8. HOST driving clock signals to the DRAM

10.2.2 Specification for DRAM Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5 SDRAM device.

[Table 15] DRAM Input Clock Jitter Specifications

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
DRAM Reference clock frequency	tCK	0.9999*f0	1.0001*f0	0.9999*f0	1.0001*f0	MHz	1,11
Duty Cycle Error	tCK_Duty_UI_Error	-	0.05	-	0.05	UI	1,4,11
Rj RMS value of 1-UI Jitter	tCK_1UI_Rj_NoBUJ	-	0.0037	-	0.0037	UI(RMS)	3,5,11
Dj pp value of 1-UI Jitter	tCK_1UI_Dj_NoBUJ	-	0.030	-	0.030	UI	3,6,11
Tj value of 1-UI Jitter	tCK_1UI_Tj_NoBUJ	-	0.090	-	0.090	UI	3,6,11
Rj RMS value of N-UI Jitter, where N=2,3	tCK_NUI_Rj_NoBUJ, where N=2,3	-	0.0040	-	0.0040	UI(RMS)	3,7,11
Dj pp value of N-UI Jitter, where N=2,3	tCK_NUI_Dj_NoBUJ, where N=2,3	-	0.074	-	0.074	UI	3,7,11
Tj value of N-UI Jitter, where N=2,3	tCK_NUI_Tj_NoBUJ, where N=2,3	-	0.140	-	0.140	UI	3,8,11
Rj RMS value of N-UI Jitter, where N=4,5,6,...,30	tCK_NUI_Rj_NoBUJ,where N=4,5,6,...,30	-	TBD	-	TBD	UI(RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	UI	3,10,11,12
Tj value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	UI	3,10,11,12

NOTE :
1) f0 = Data Rate/2, example: if data rate is 4800MT/s, then f0=2400
2) Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock
3) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
4) Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI
5) Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6) Dj pp value of 1-UI jitter(after software assisted DCC).Without BUJ,but on-die system like noise present.Dj indicates Djdd of dual-Dirac fitting,after software correction of DCD
7) Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
8) Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9) Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
10) Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11) The validation methodology for these parameters will be covered in future ballots
12) If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

10.3 Differential Input Clock (CK_t, CK_c) Cross Point Voltage (VIX)

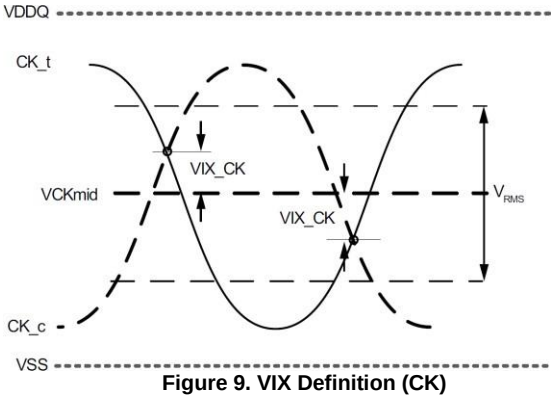


Figure 9. VIX Definition (CK)

[Table 16] Crosspoint Voltage (VIX) for Differential Input Clock

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Note
		min	max	min	max		
Clock differential input crosspoint voltage ratio	VIX_CK_Ratio	-	50	-	50	%	1,2,3

NOTE :

1) The VIX_CK voltage is referenced to VCKmid(mean) = (CK_t voltage + CK_c voltage) /2, where the mean is over 8 UI
2) VIX_CK_Ratio = (|VIX_CK| / |V_{RMS}|)*100%, where V_{RMS} = RMS(CK_t voltage - CK_c voltage)
3) Only applies when both CK_t and CK_c are transitioning

10.4 Differential Input Clock Voltage Sensitivity

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock by varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise. This specifies the Rx voltage sensitivity requirement. The system input swing to the DRAM must be larger than the DRAM Rx at the specified BER.

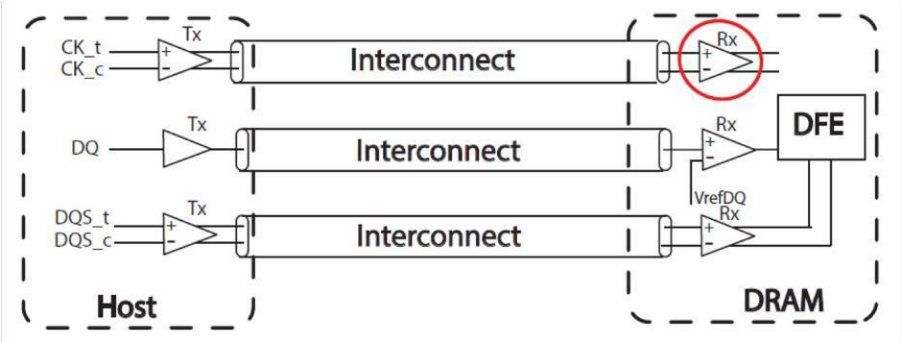


Figure 10. Example of DDR5 Memory Interconnect

10.4.1 Differential Input Clock Voltage Sensitivity Parameter

Differential input clock (CK_t, CK_c) VRx_CK is defined and measured as shown below. The clock receiver must pass the minimum BER requirements for DDR5.

[Table 17] Differential Input Clock Voltage Sensitivity Parameter

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Note
		min	max	min	max		
Input Clock Voltage Sensitivity (differential pp)	VRx_CK	-	180	-	160	mV	1,2

NOTE :
1) Refer to the minimum BER requirements for DDR5.
2) The validation methodology for this parameter will be covered in future ballot(s).

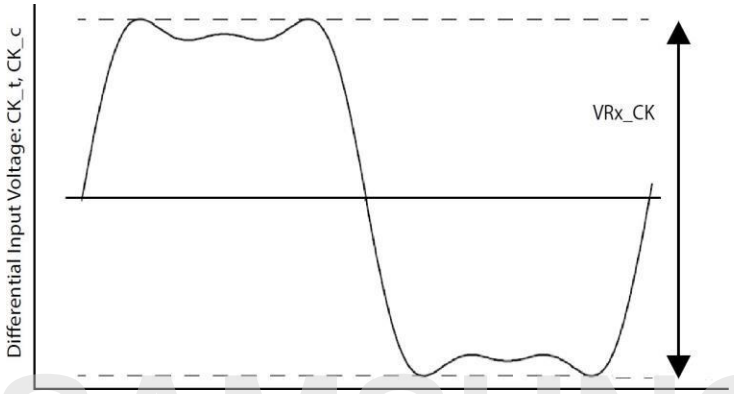


Figure 11. VRx_CK

10.4.2 Differential Input Voltage Levels for Clock

[Table 18] Differential Clock (CK_t, CK_c) Input Levels

From	Parameter	DDR5-4400	DDR5-4800	Note
$V_{IHdiff}CK$	Differential input high measurement level (CK_t, CK_c)	0.75 x $V_{diffpk-pk}$	0.75 x $V_{diffpk-pk}$	1,2
$V_{ILdiff}CK$	Differential input low measurement level (CK_t, CK_c)	0.25 x $V_{diffpk-pk}$	0.25 x $V_{diffpk-pk}$	1,2

NOTE :
1) $V_{diffpk-pk}$ defined in Figure 12.
2) $V_{diffpk-pk}$ is the mean high voltage minus the mean low voltage over TBD samples.
3) All parameters are defined over the entire clock common mode range.

10.4.3 Differential Input Slew Rate Definition for Clock (CK_t, CK_c)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown below.

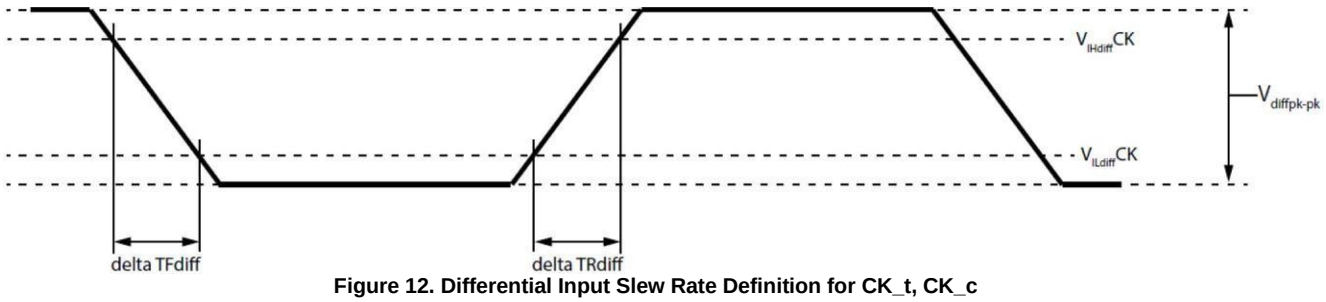


Figure 12. Differential Input Slew Rate Definition for CK_t, CK_c

[Table 19] Differential Input Slew Rate Definition for CK_t, CK_c

Parameter	Measured		Defined by	Note
	From	To		
Differential Input slew rate for rising edge (CK_t - CK_c)	$VIL_{diff}CK$	$VIH_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) /deltaTRdiff	
Differential Input slew rate for falling edge (CK_t - CK_c)	$VIH_{diff}CK$	$VIL_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) /deltaTFdiff	

[Table 20] Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Note
		min	max	min	max		
Differential Input Slew Rate for CK_t, CK_c	SRIdiff_CK	2	14	2	14	V/ns	

10.5 Rx DQS Jitter Sensitivity

The receiver DQS jitter sensitivity test provides the methodology for testing the receiver's strobe sensitivity to an applied duty cycle distortion (DCD) and/ or random jitter (Rj) at the forwarded strobe input without adding jitter, noise and ISI to the data. The receiver must pass the appropriate BER rate when no cross-talk nor ISI is applied, and must pass through the combination of applied DCD and Rj.

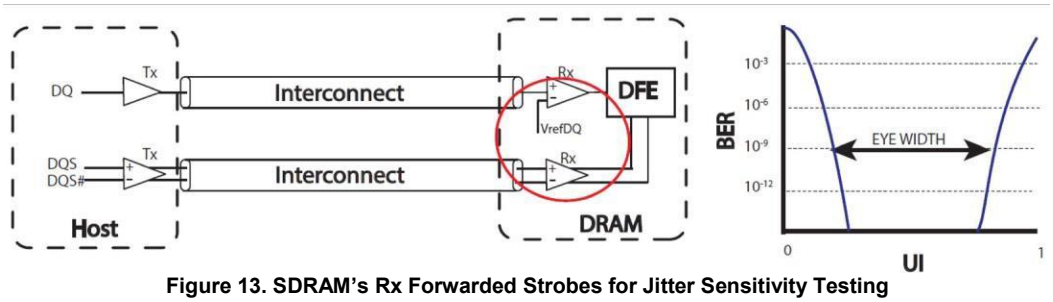


Figure 13. SDRAM's Rx Forwarded Strobes for Jitter Sensitivity Testing

10.5.1 Rx DQS Jitter Sensitivity Specification

The following table provides Rx DQS Jitter Sensitivity Specification for the DDR5 DRAM receivers when operating at various possible transfer rates. These parameters are tested on the CTC2 card without Rx Equalization set. Additive DFE Gain Bias can be set.

[Table 21] Rx DQS Jitter Sensitivity Specification

[BER = Bit Error Rate; DCD = Duty Cycle Distortion; Rj =Random Jitter]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Note
		min	max	min	max		
DQ Timing Width	tRx_DQ_tMargin	0.825	-	0.825	-	UI	1,2,3,8,9,10
Degradation of timing width compared to tRx_DQ_tMargin, with DCD injection in DQS	△ tRx_DQ_tMargin_DQS_DCD	-	0.06	-	0.06	UI	1,4,8,9,10
Degradation of timing width compared to tRx_DQ _tMargin, with Rj injection in DQS	△ tRx_DQ_tMargin_DQS_Rj	-	0.09	-	0.09	UI	1,5,8,9,10
Degradation of timing width compared to tRx_DQ_tMargin, with both DCD and Rj injection in DQS	△ tRx_DQ_tMargin_DQS_DCD_Rj	-	0.15	-	0.15	UI	1,2,6,8,9,10
Delay of any data lane relative to the DQS_t DQS_c crossing	tRx_DQS2DQ	1	3.25	1	3.5	UI	1,7,8,9,10

NOTE :

1) Validation methodology will be defined in future JEDEC ballots. 2UI is defined as 1tCK for this parameter.
2) Each of ?tRx_DQ_tMargin_DQS_DCD, ?tRx_DQ_tMargin_DQS_Rj, and ?tRx_DQ_tMargin_DQS _DCD_Rj can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by 5% or more.
3) DQ Timing Width - timing width for any data lane using repetitive patterns (check note 4 for the pattern) measured at BER=E-9.
4) Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 "1s" and 3 "0s".
5) Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing
6) Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.
7) Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
8) All measurements at BER=E-9.
9) This test should be done after the DQS and DQ Voltage Sensitivity tests are completed and passing.
10) The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

10.5.2 Test Conditions for Rx DQS Jitter Sensitivity Tests

Table 22 lists the amount of Duty Cycle Distortion (DCD) and/or Random Jitter (Rj) that must be applied to the forwarded strobe when measuring the Rx DQS Jitter Sensitivity parameters specified in Table 21.

[Table 22] Test Conditions for Rx DQS Jitter Sensitivity Testing

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Applied DCD to the DQS	tRx_DQS_DCD	-	0.045	-	0.045	UI	1,2,3,6,7,10
Applied Rj RMS to the DQS	tRx_DQS_Rj	-	0.0075	-	0.0075	UI (RMS)	1,2,4,6,8,10
Applied DCD and Rj RMS to the DQS	tRx_DQS_DCD_Rj	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	UI	1,2,5,6,7,9,10

NOTE :

1) While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
2) The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin.
3) Various DCD values should be tested, complying within the maximum limits.
4) Various Rj values should be tested, complying within the maximum limits.
5) Various combinations of DCD and Rj should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of these injected jitter is specified in a separate table.
6) Although DDR5 has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 “1s” and 3 “0s” is used for this test.
7) Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI).
8) RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
9) Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
10) The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

10.6 Rx DQS Voltage Sensitivity

10.6.1 Overview

The receiver DQS (strobe) input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

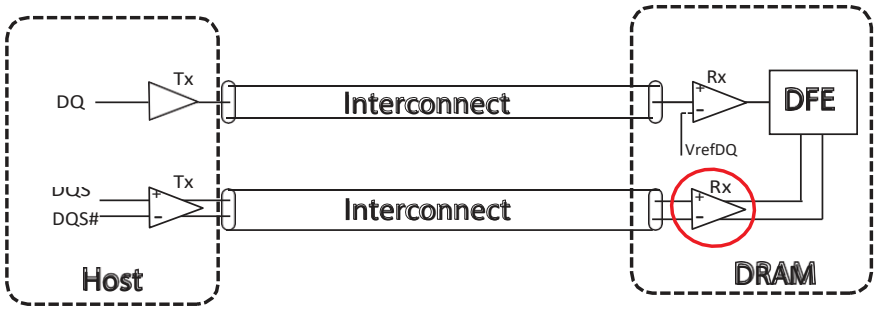


Figure 14. Example of DDR5 Memory Interconnect

10.6.2 Receiver DQS Voltage Sensitivity Parameter

Input differential (DQS_t, DQS_c) VRx_DQS is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

[Table 23] Rx DQS Input Voltage Sensitivity Parameter

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
DQS Rx Input Voltage Sensitivity (differential pp)	VRx_DQS	-	100	-	100	mV	1,2,3

NOTE :
1) Refer to the minimum BER requirements for DDR5.
2) The validation methodology for this parameter will be covered in future ballot(s).
3) Test using clock like pattern of repeating 3 "1s" and 3 "0s".

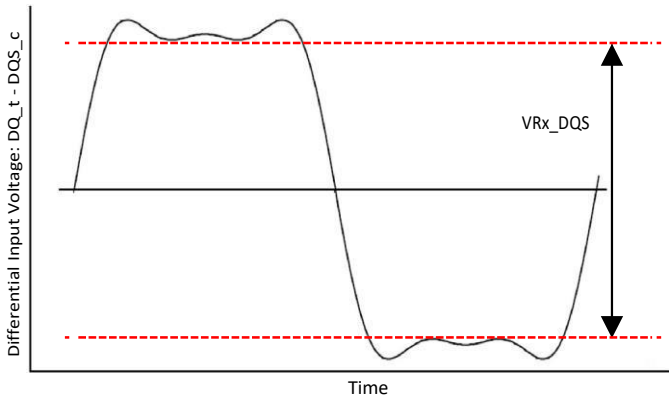


Figure 15. VRx_DQS

10.7 Differential Strobe (DQS_t, DQS_c) Input Cross Point Voltage (VIX)

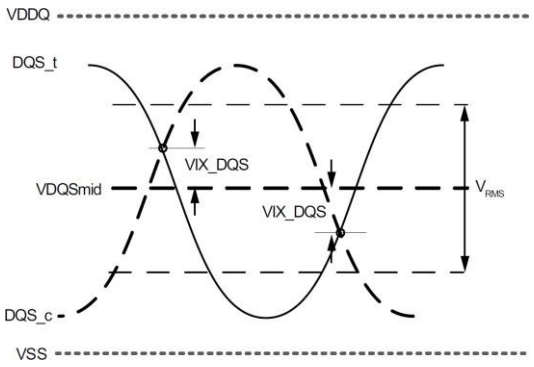


Figure 16. VIX Definition (DQS)

[Table 24] Crosspoint Voltage (VIX) for DQS Differential Input Signals

Parameter	Symbol	DDR5-4400	DDR5-4800	Unit	Note
DQS differential input crosspoint voltage ratio	VIX_DQS_Ratio	50	50	%	1,2

NOTE :
1) The VIX_DQS voltage is referenced to VDQSmid(mean) = (DQS_t voltage + DQS_c voltage) /2, where the mean is over 8 UI
2) VIX_DQS_Ratio = (|VIX_DQS| / |VRMS|)*100%, where VRMS = RMS(DQS_t voltage - DQS_c voltage)
3) Only applies when both DQS_t and DQS_c are transitioning (including preamble)

10.8 Rx DQ Voltage Sensitivity

10.8.1 Overview

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

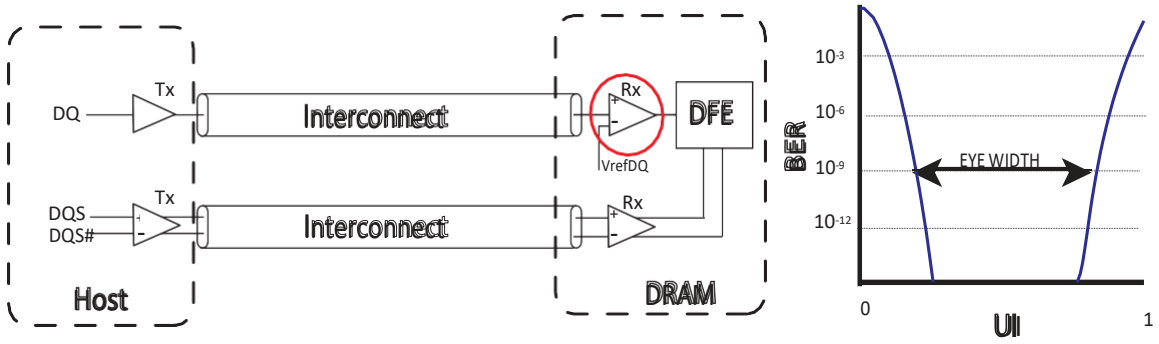


Figure 17. Example of DDR5 Memory Interconnect

10.8.2 Receiver DQ Input Voltage Sensitivity Parameters

Input single-ended VRx_DQ is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

[Table 25] Rx DQ Input Voltage Sensitivity Parameters

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Minimum DQ Rx input voltage sensitivity applied around Vref	VRx_DQ	-	65	-	65	mV	1,2,3

NOTE :
1) Refer to the minimum BER requirements for DDR5
2) The validation methodology for this parameter is TBD
3) Recommend testing using clock like pattern such as repeating 3 "1s" and 3 "0s"

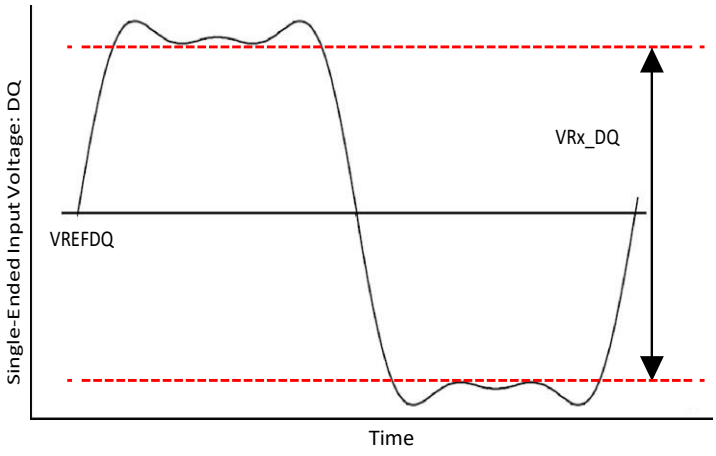


Figure 18. VRx_DQ

10.8.3 Differential Input Levels for DQS

[Table 26] Differential Input Levels for DQS (DQS_t, DQS_c)

From	Parameter	DDR5-4400	DDR5-4800	Note
$V_{IHdiff}DQS$	Differential input high measurement level (DQS_t, DQS_c)	0.75 x $V_{diffpk-pk}$	0.75 x $V_{diffpk-pk}$	1,2,3
$V_{ILdiff}DQS$	Differential input low measurement level (DQS_t, DQS_c)	0.25 x $V_{diffpk-pk}$	0.25 x $V_{diffpk-pk}$	1,2,3

NOTE :
1) Vdiffpk-pk defined in Figure 17
2) Vdiffpk-pk is the mean high voltage minus the mean low voltage over TBD samples
3) All parameters are defined over the entire clock common mode range

10.8.4 Differential Input Slew Rate for DQS_t, DQS_c

Input slew rate for differential signals are defined and measured as shown below.

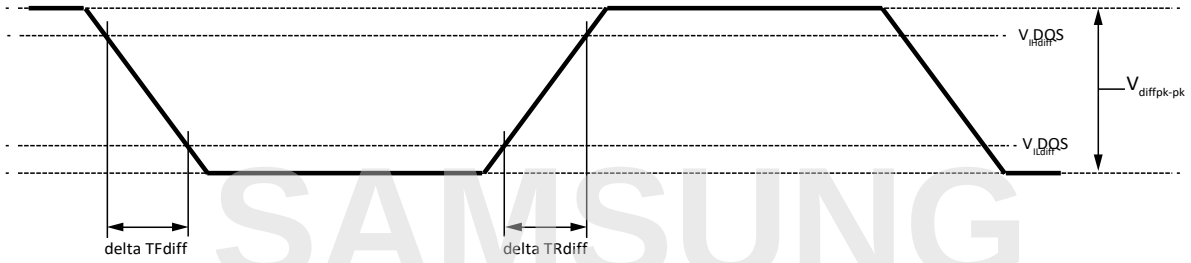


Figure 19. Differential Input Slew Rate Definition for DQS_t, DQS_c

[Table 27] Differential Input Slew Rate Definition for DQS_t, DQS_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (DQS_t, DQS_c)	$V_{ILdiff}DQS$	$V_{IHdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) / deltaTRdiff	
Differential Input slew rate for falling edge (DQS_t, DQS_c)	$V_{IHdiff}DQS$	$V_{ILdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) / deltaTFdiff	

[Table 28] Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	DDR5-4400	DDR5-4800	Unit	Notes
Differential Input Slew Rate for DQS_t, DQS_c	SRIdiff_DQS	TBD	TBD	V/ns	1

NOTE :
1) Only applies when both DQS_t and DQS_c are transitioning.

10.9 Rx Stressed Eye

The stressed eye tests provide the methodology for creating the appropriate stress for the DRAM's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk

.

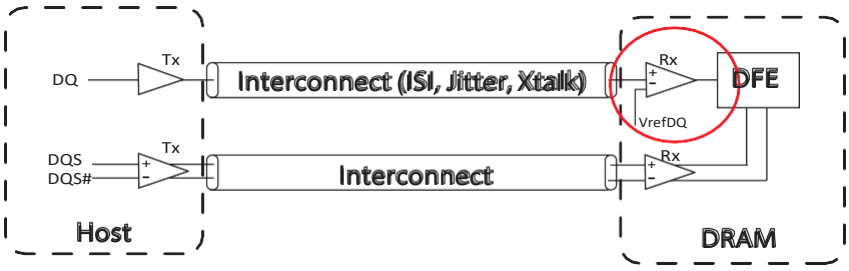


Figure 20. Example of Rx Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk

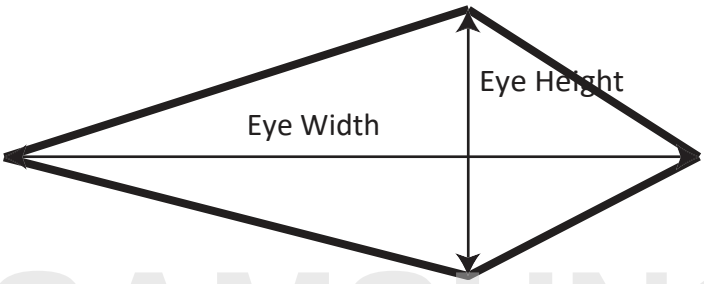


Figure 21. Example of Rx Stressed Eye Height and Eye Width

10.9.1 Parameters for DDR5 Rx Stressed Eye Tests

[Table 29] Test Conditions for Rx Stressed Eye Tests

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Eye height of stressed eye for Golden Reference Channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	-	75	-	70	mV	1,2,3,4,5,6,7,8,9,10
Eye width of stressed eye Golden Reference Channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	-	0.25	-	0.25	UI	1,2,3,4,5,6,7,8,9,10
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	mV	1.2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	0	0.45	0	0.45	UI p-p	1,2
Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	mV p-p	1,2
Golden Reference Channel 1 Characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics	TBD	TBD	TBD	TBD	dB	3

NOTE :

1) Must meet minimum BER of 1E-16 or better requirement with the stressed eye at the slice of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER E-9 and extrapolating to BER E-16.
2) These parameters are applied on the defined golden reference channel with parameters TBD.
3) DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 shall be less than 60mV ($|Tap\text{-}2| + |Tap\text{-}3| + |Tap\text{-}4| < 60mV$).
4) Evaluated with no DC supply voltage drift.
5) Evaluated with no temperature drift.
6) Supply voltage noise limited according to DC bandwidth spec, see DC Operating Conditions
7) The stressed eye is to be assumed to have a diamond shape
8) The VREFDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test, including the limits placed in Note 3.
9) The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, VrefDQ, and DFE solution to give the best eye margin.

10.10 Connectivity Test Mode - Input level and Timing Requirement

During CT Mode, input levels are defined below.
TEN pin: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ
CS_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
Test Input pins: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
RESET_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK_t and CK_c signals will be ignored and the DDR5 memory device will enter into the CT mode after time tCT_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on, after RESET_n has de-asserted, the wait time after the RESET_n de-assertion has elapsed, and prior to starting clocks (CK_t, CK_c).

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR5 memory device are unknown and the integrity of the original content of the memory array is not guaranteed; therefore, the reset initialization sequence is required.

All output signals at the test output pins will be stable within tCT_valid after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained High and Low respectively.

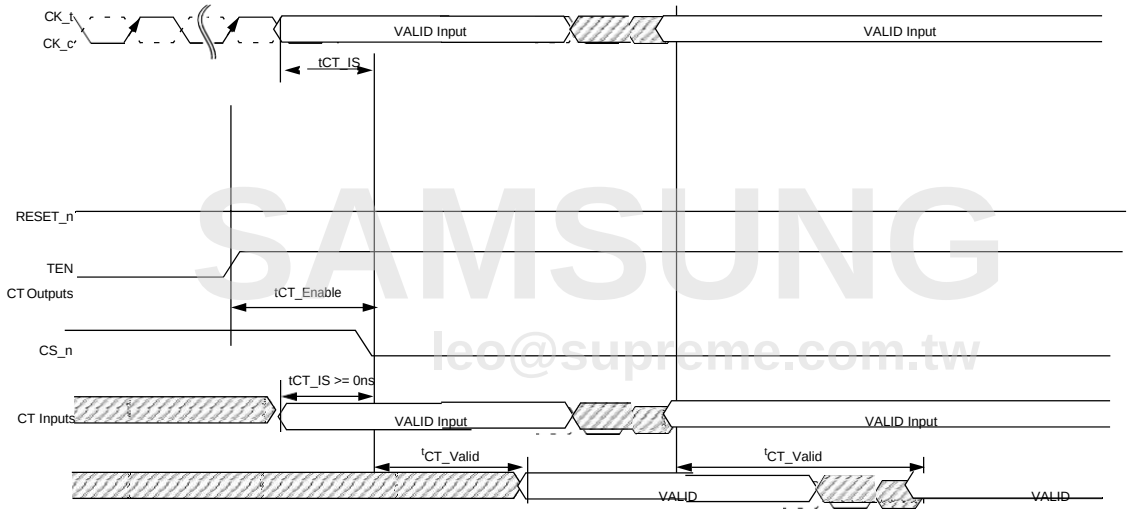


Figure 22. Timing Diagram for Connectivity Test (CT) Mode

[Table 30] AC parameters for Connectivity Test (CT) Mode

Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_Valid	-	200	ns

10.10.1 Connectivity Test (CT) Mode Input Levels

Following input parameters will be applied for DDR5 SDRAM Input Signals during Connectivity Test Mode.

[Table 31] CMOS rail to rail Input Levels for TEN, CS_n and Test inputs

Parameter	Symbol	Min	Max	Unit	Notes
TEN AC Input High Voltage	VIH(AC)_TEN	0.8 * VDDQ	VDDQ	V	1
TEN DC Input High Voltage	VIH(DC)_TEN	0.7 * VDDQ	VDDQ	V	
TEN DC Input Low Voltage	VIL(DC)_TEN	VSS	0.3 * VDDQ	V	
TEN AC Input Low Voltage	VIL(AC)_TEN	VSS	0.2 * VDDQ	V	2
TEN Input signal Falling time	TF_input_TEN	-	10	ns	
TEN Input signal Rising time	TR_input_TEN	-	10	ns	

NOTE :
1) Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
2) Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

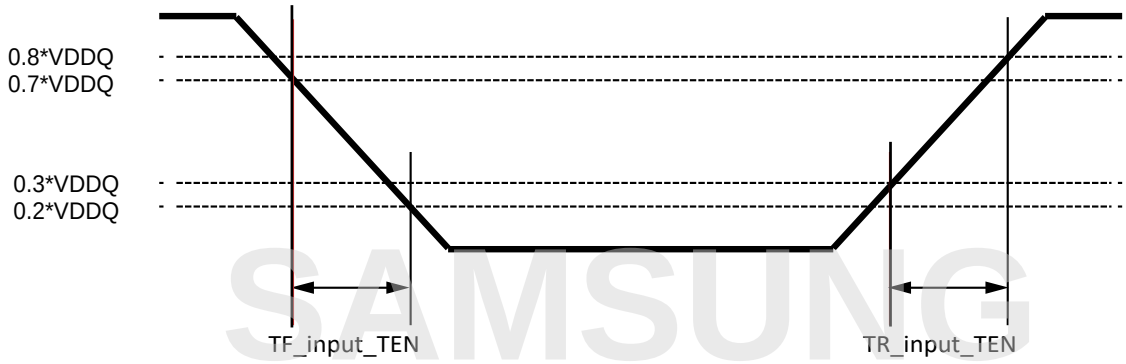


Figure 23. TEN Input Slew Rate Definition

10.10.2 CMOS rail to rail Input Levels for RESET_n

[Table 32] CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDDQ	VDDQ	V	5
DC Input High Voltage	VIH(DC)_RESET	0.7*VDDQ	VDDQ	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDDQ	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDDQ	V	6
Rising time	TR_RESET	-	1.0	us	
RESET pulse width	tPW_RESET	1.0	-	us	3,4

NOTE :
1) After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2) Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3) RESET is destructive to data contents.
4) This definition is applied only for “Reset Procedure at Power Stable”.
5) Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
6) Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

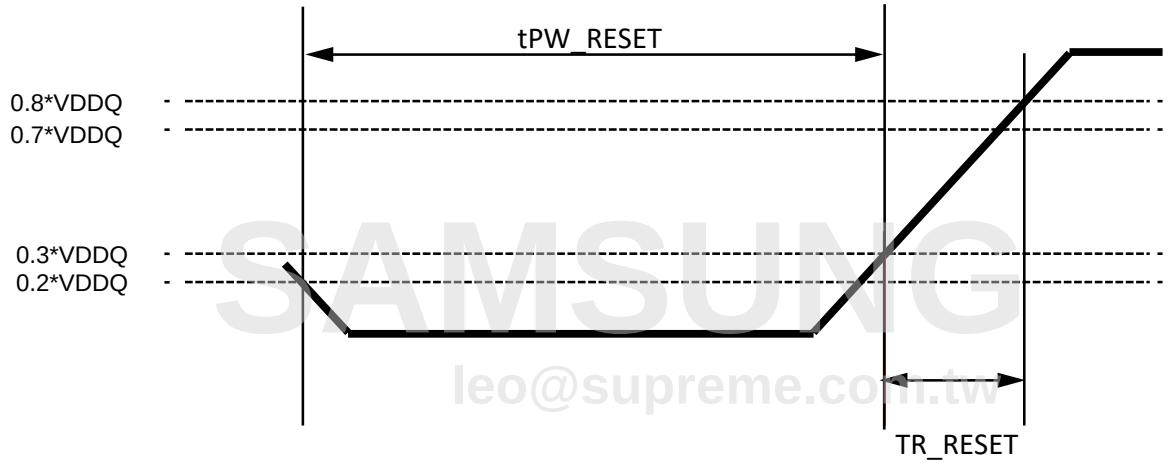


Figure 24. RESET_n Input Slew Rate Definition

11.0 AC&DC OUTPUT MEASUREMENT LEVELS and TIMING

11.1 Output Driver DC Electrical Characteristics for DQS and DQ

The DDR5 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below.

Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

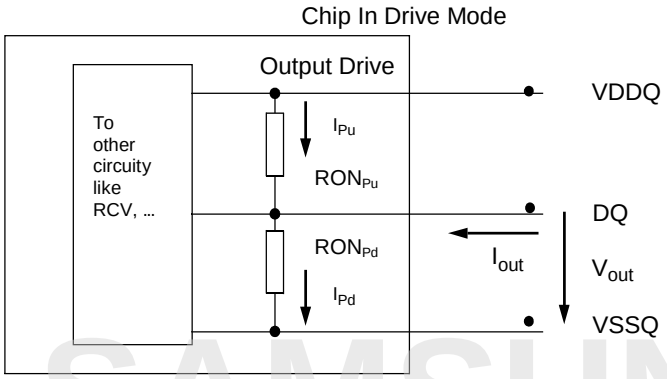


Figure 25. Output Driver Impedance Ron

[Table 33] Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE :

1) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity (TBD).
2) Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.
3) Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value.

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4) RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

5) This parameter of x16 device is specified for Upper byte and Lower byte.

11.2 Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ

The DDR5 Loopback driver supports 34 ohms. A functional representation of the output buffer is shown in the figure below.

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\,out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\,out|}$$ under the condition that RON_{Pu} is off

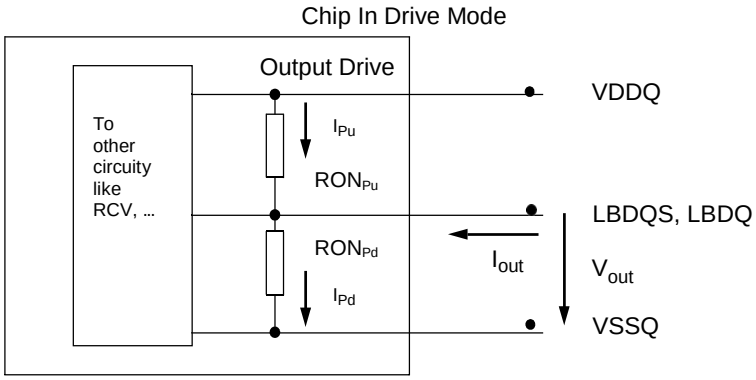


Figure 26. Output Driver for Loopback Signals

[Table 34] Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch LBDQS-LBDQ within device variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch LBDQS-LBDQ within device variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE :

1) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2) Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.
3) Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4) RON variance range ratio to RON Nominal value in a given component, including LBDQS and LBDQ

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

11.3 Loopback Output Timing

Loopback strobe LBDQS to Loopback data LBDQ relationship is illustrated inFigure 27.
- tLBQSH describes the single-ended LBDQS strobe high pulse width.
- tLBQSL describes the single-ended LBDQS strobe low pulse width.
- tLBDQSQ describes the latest valid transition of LBDQ measured at both rising and falling edges of LBDQS.
- tLBQH describes the earliest invalid transition of LBDQ measured at both rising and falling edges of LBDQS.
- tLBDVW describes the data valid window per device per UI and is derived from (tLBQH-tLBDQSQ) of each UI on a given DRAM.

[Table 35] Loopback Output Timing Parameters

Speed		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Loopback Timing							
Loopback LBDQS Output Low Time	tLBQSL	0.7	-	0.7	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	0.7	-	0.7	-	tCK	1
Loopback LBDQS to LBDQ Skew	tLBDQSQ	0.2	-	0.2	-	tCK/2	1
Loopback LBDQ Output Time from LBDQS	tLBQH	3.6	-	3.6	-	tCK/2	1
Loopback Data valid window (tLBQH-tLBDQSQ) of each UI per DRAM	tLBDVW	3.4	-	3.4	-	tCK/2	1

NOTE :
1) Based on Loopback 4-way interleave setting (see MR53).

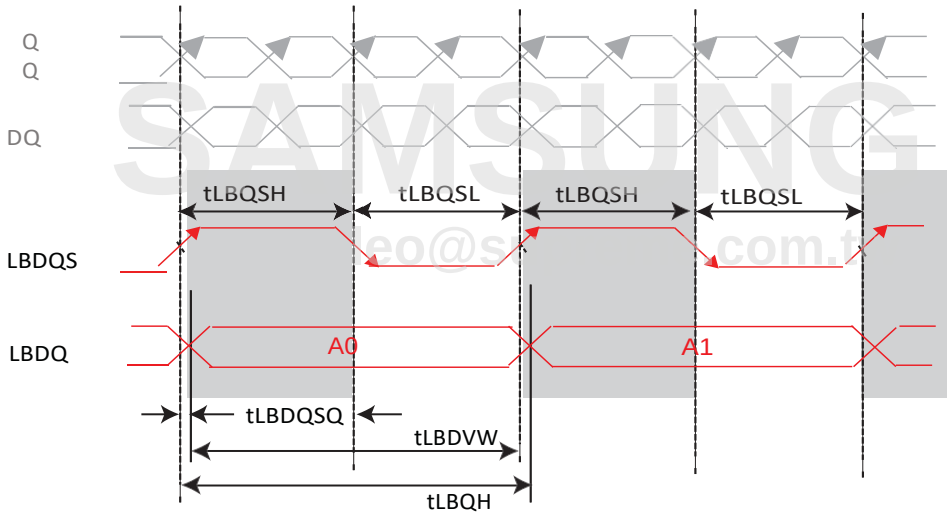


Figure 27. Loopback Strobe to Data Relationship

11.3.1 Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{I\ Iout\ I}$$ under the condition that RON_{Pu} is off

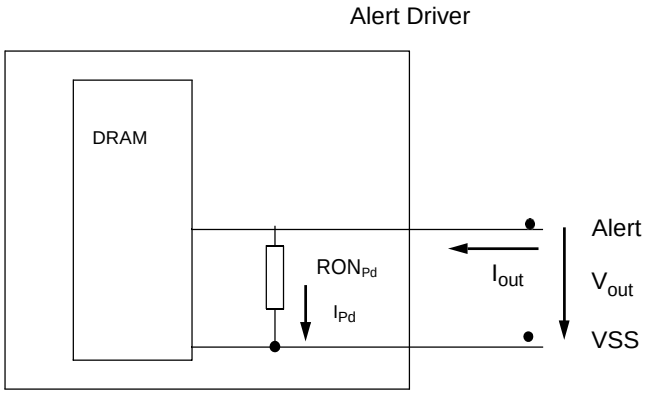


Figure 28. Alert Driver

Resistor	Vout	Min	Max	Unit	Notes
RON_{Pd}	VOLdc= 0.1* VDDQ	0.3	1.1	$R_{ZQ}/7$	
	V_{OMdc} = 0.8* VDDQ	0.4	1.1	$R_{ZQ}/7$	
	V_{OHdc} = 0.95* VDDQ	0.4	1.25	$R_{ZQ}/7$	

11.3.2 Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied to the Test Output Pin during Connectivity Test (CT) Mode.
The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ}-V_{OUT}}{|Iout|}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|Iout|}$$

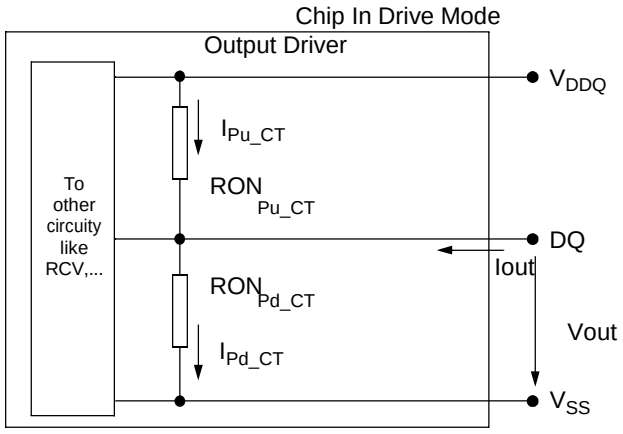


Figure 29. Output Driver

RONNOM_CT	Resistor	Vout	Max	Units	NOTE
34Ω	RONPd_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2
	RONPu_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2

NOTE :
1) Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined
2) Uncalibrated drive strength tolerance is specified at +/- 30%

11.4 Single-ended Output Levels - VOL/VOH

[Table 36] Single-ended Output levels

Symbol	Parameter	DDR5-4400	DDR5-4800	Units	Notes
VOH	Output high measurement level (for output SR)	0.75 x Vpk-pk	0.75 x Vpk-pk	V	1
VOL	Output low measurement level (for output SR)	0.25 x Vpk-pk	0.25 x Vpk-pk	V	1

NOTE :
1) $V_{pk-pk}$is the mean high voltage minus the mean low voltage over TBD samples.

11.5 Single-Ended Output Levels - VOL/VOH for Loopback Signals

[Table 37] Single-ended Output levels for Loopback Signals

Symbol	Parameter	DDR5-4400	DDR5-4800	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	0.25 x V_{pk-pk}	V	1

NOTE :
1) $V_{pk-pk}$is the mean high voltage minus the mean low voltage over TBD samples.

11.6 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL and VOH for single ended signals as shown in Table 38 and Figure 30.

[Table 38] Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}	V_{OH}	[V_{OH}-V_{OL}] / delta TRse
Single ended output slew rate for falling edge	V_{OH}	V_{OL}	[V_{OH}-V_{OL}] / delta TFse

NOTE :
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

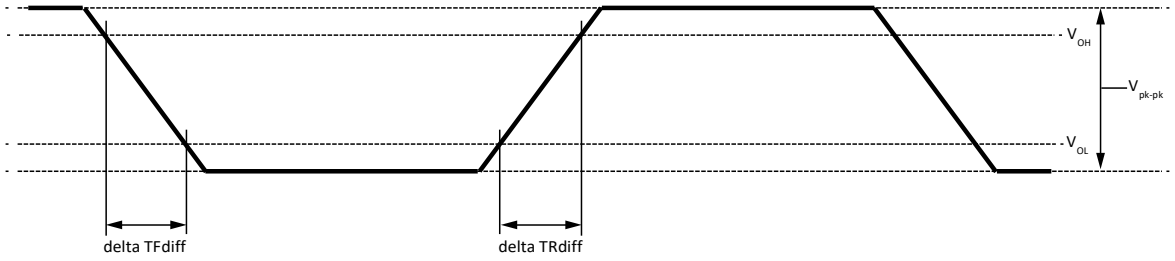


Figure 30. Single-ended Output Slew Rate Definition

[Table 39] Single-ended Output Slew Rate

Speed		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Single ended output slew rate	SRQse	8	24	8	24	V/ns	

11.7 Differential Output Levels

[Table 40] Differential Output levels

Symbol	Parameter	DDR5-4400	DDR5-4800	Units	Notes
V_{OHdiff}	Differential output high measurement level (for output SR)	0.75 x $V_{diffpk-pk}$	0.75 x $V_{diffpk-pk}$	V	1
V_{OLdiff}	Differential output low measurement level (for output SR)	0.25 x $V_{diffpk-pk}$	0.25 x $V_{diffpk-pk}$	V	1

NOTE :
1) $V_{diffpk-pk}$is the mean high voltage minus the mean low voltage over TBD samples.

11.8 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff and VOHdiff for differential signals as shown in Table 41 and Figure 31.

[Table 41] Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}	V_{OHdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}	V_{OLdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TFdiff

NOTE :
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

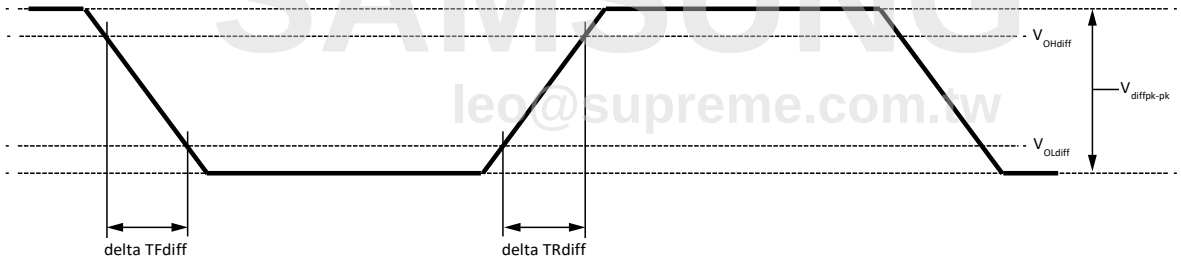


Figure 31. Differential Output Slew Rate Definition

[Table 42] Differential Output Slew Rate

Speed		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Differential output slew rate	SRQdiff	16	48	16	48	V/ns	

11.9 Tx DQS Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 43.

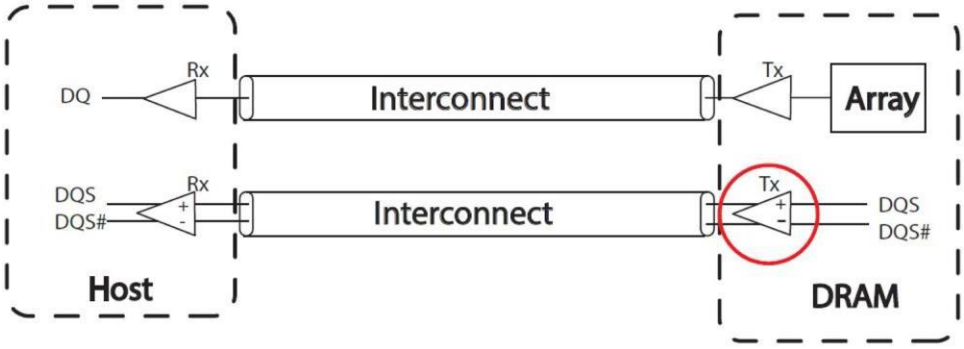


Figure 32. Tx DQS Jitter

11.9.1 Tx DQS Jitter Parameters

[Table 43] Tx DQS Jitter Parameters

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Rj RMS Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,4,5,6,7,8,9,10,11,12
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj_NoBUJ	-	0.150	-	0.150	UI	1,2,3,5,6,7,8,9,10,11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 4	tTx_DQS_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,5,6,7,8,9,10,11,12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 4	tTx_DQS_NUI_Dj_NoBUJ	-	0.150	-	0.150	UI	1,2,3,5,6,7,8,9,10,11

NOTE :

1) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all thetransmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
2) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3) The validation methodology for these parameters will be covered in future ballots
4) Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction ofDCD
5) See Chapter 12 for details on the minimum BER requirements
6) See Chapter 12 for details on UI, NUI and Jitter definitions
7) Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running the Tx DQ Jitter test
8) The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44, and the Mode Registers for the Per Pin DCA of DQS are MR103 - MR110
9) Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test
10) These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature
11) Tested on the CTC2 card only
12) The max value of tTx_DQS_Rj_1UI_NoBUJ and tTx_DQS_Rj_NUI_NoBUJ can be 6mUI RMS

11.10 Tx DQ Jitter

11.10.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 44.

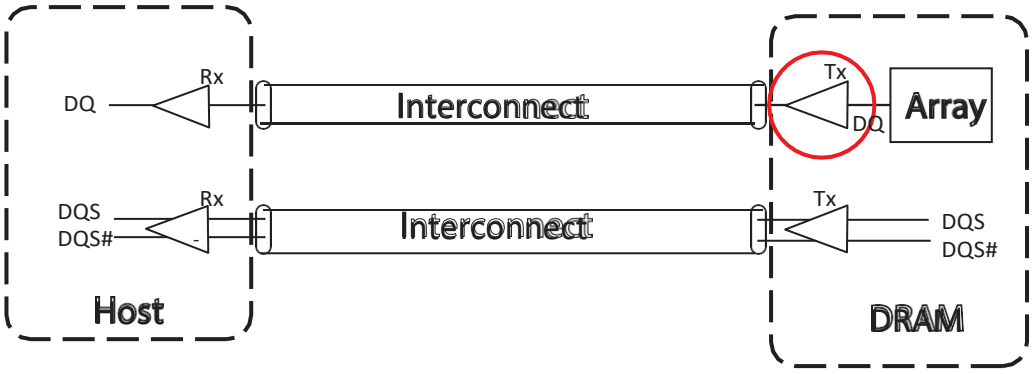


Figure 33. Tx DQ Jitter

11.10.2 Tx DQ Jitter Parameters

[Table 44] Tx DQ Jitter Parameters

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Rj RMS of 1-UI jitter without BUJ	tTx_DQS_1UI_Rj_No BUJ	-	tCK_1UI_Rj_ NoBUJ + 0.002	-	tCK_1UI_Rj_ NoBUJ + 0.002	UI (RMS)	1,3,4,5,7,8,9,10, 11,12,13,14
Dj pp 1-UI jitter without BUJ	tTx_DQS_1UI_Dj_No BUJ	-	0.150	-	0.150	UI	3,5,7,8,9,10,11, 12,13
Rj RMS of N-UI jitter without BUJ, where 1<N<4	tTx_DQS_NUI_Rj_No BUJ	-	tCK_NUI_Rj_ NoBUJ + 0.002	-	tCK_NUI_Rj_ NoBUJ + 0.002	UI (RMS)	3,5,7,8,9,10,11, 12,13,14
Dj pp N-UI jitter without BUJ, where 1<N<4	tTx_DQS_NUI_Dj_No BUJ	-	0.150	-	0.150	UI	3,6,7,8,9,10,11, 12,13
Delay of any data lane relative to strobe lane	tTx_DQS2DQ	-0.100	0.100	-0.100	0.100	UI	3,5,6,7,9,10,11, 12,13

NOTE :

1) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmittermeasurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all thetransmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant.To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
2) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When asocket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
3) The validation methodology for these parameters will be covered in future ballots
4) Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD.
5) Delay of any data lane relative to strobe lane, as measured at Tx output.
6) Vref noise level to DQ jitter should be adjusted to minimize DCD.
7) See Chapter 12 for details on the minimum BER requirements.
8) See Chapter 12 for details on UI, NUI and Jitter definitions.
9) Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test.
10) The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where 0≤x≤7, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where 0≤y≤7.
11) Spread Spectrum Clocking (SSC) must be disabled while running this test.
12) These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.
13) Tested on the CTC2 card only.
14) The max value of tTx_DQ_Rj_1UI_NoBUJ and tTx_DQ_Rj_NUI_NoBUJ can be 6mUI RMS.

11.11 Tx DQ Stressed Eye

Tx DQ stressed eye height and eye width must meet minimum specification values at BER=E^{-9} and confidence level 99.5%. Tx DQ Stressed Eye shows the DQS to DQ skew for both Eye Width and Eye Height. In order to support different Host Receiver (Rx) designs, it is the responsibility of the Host to insure the advanced DQS edges are adjusted accordingly via the Read DQS Offset Timing mode register settings (MR40 OP[3:0]).

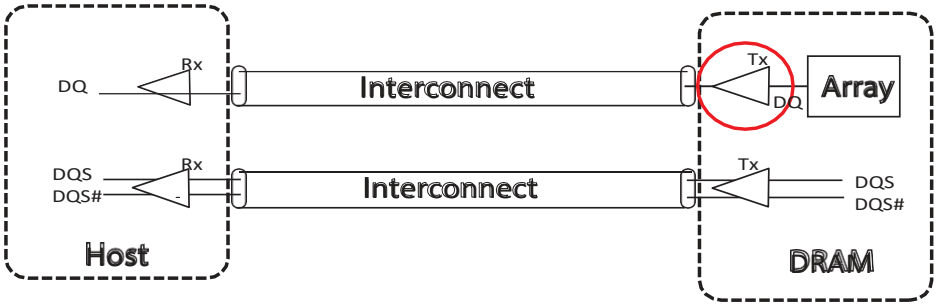


Figure 34. Example of DDR5 Memory Interconnect

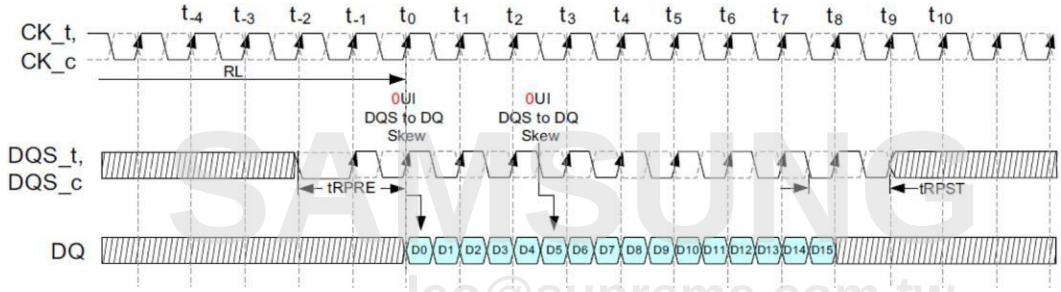


Figure 35. Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 0 UI skew

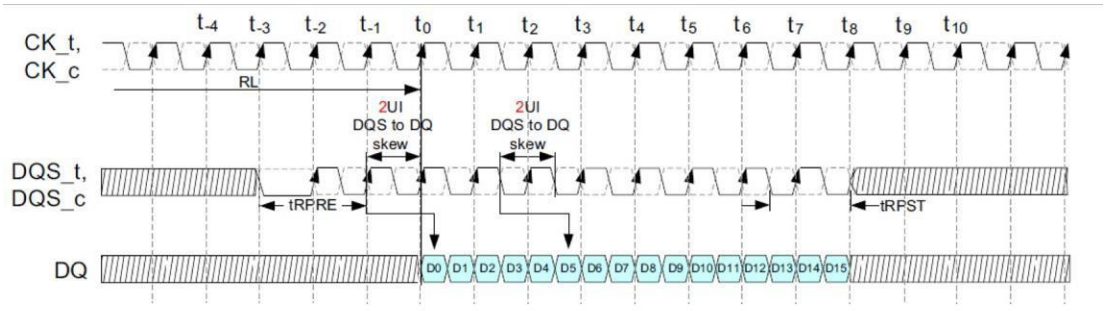


Figure 36. Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 2 UI skew with Read DQS Offset Timing set to 1 Clock (2UI)

11.11.1 Tx DQ Stressed Eye Parameters

[Table 45] Tx DQ Stressed Eye Parameters

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate, SES=Stressed Eye Skew]

Parameter	Symbol	DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max		
Eye Height specified at the transmitter with a skew between DQ and DQS of 1UI	TxEH_DQ_SES_1UI	TBD	-	TBD	-	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 1UI	TxEW_DQ_SES_1UI	0.72	-	0.72	-	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 2UI	TxEH_DQ_SES_2UI	TBD	-	TBD	-	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 2UI	TxEW_DQ_SES_2UI	0.72	-	0.72	-	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 3UI	TxEH_DQ_SES_3UI	TBD	-	TBD	-	mV	1,2,3,4,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 3UI	TxEW_DQ_SES_3UI	0.72	-	0.72	-	UI	1,2,3,4,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 4UI	TxEH_DQ_SES_4UI	TBD	-	TBD	-	mV	1,2,3,4,5,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 4UI	TxEW_DQ_SES_4UI	TBD	-	TBD	-	UI	1,2,3,4,5,6,7,8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 5UI	TxEH_DQ_SES_5UI	TBD	-	TBD	-	mV	1,2,3,4,5,6,7,8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 5UI	TxEW_DQ_SES_5UI	TBD	-	TBD	-	UI	1,2,3,4,5,6,7,8,9,10

NOTE :

1) Minimum BER E-9 and Confidence Level of 99.5% per pin
2) Refer to the minimum Bit Error Rate (BER) requirements for DDR5
3) The validation methodology for these parameters is TBD
4) Mismatch is defined as DQS to DQ mismatch, in UI increments
5) The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable
6) Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test
7) The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQS are MR103-MR110, the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where 0≤x≤7, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where 0≤y≤7.
8) Spread Spectrum Clocking (SSC) must be disabled while running this test
9) These parameters are tested using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.
10) Tested on the CTC2 card only
11) Matched DQS to DQ would require the DQs to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI mismatch would require the DQS to be adjusted 1.5UI. Generally, for XUI mismatch the DQ must be adjusted XUI + 0.5UI to be placed in the center of the eye

12.0 SPEED BIN

[Table 46] DDR5-4400 Speed Bins and Operations

Speed Bin					DDR5-4400		Unit	NOTE
CL-nRCD-nRP					36-36-36			
Parameter				Symbol	min	max		
Read command to first data				tAA	16.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS+tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL	CL-2		nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns) [5]	Read [12] CL	Supported Frequency Down Bins				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681		
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681		
3200AN	15.000	15.000	24	tCK(AVG)	RESERVED			
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED		ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555		
4000BN,B	18.000	16.000	32	tCK(AVG)	0.500	<0.555		
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED			
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	ns	
4400N	14.545	14.545	32	tCK(AVG)	RESERVED		ns	
Supported CL					22,26,28,30,32,36,40		nCK	

[Table 47] DDR5-4800 Speed Bins and Operations

Speed Bin					DDR5-4800		Unit	NOTE
CL-nRCD-nRP					40-39-39			
Parameter				Symbol	min	max		
Read command to first data				tAA	16.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC	48.000		ns	7,8
CAS Write Latency				CWL	CL-2		nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681		
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681		
3200AN	15.000	15.000	24	tCK(AVG)	RESERVED			
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED		ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555		
4000BN,B	18.000	16.000	32	tCK(AVG)	0.500	<0.555		
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED			
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	ns	
4400N	14.545	14.545	32	tCK(AVG)	RESERVED		ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	ns	
4800BN,B	16.666	16.666	40	tCK(AVG)	0.416	<0.454	ns	
4800AN	16.666	16.250	40	tCK(AVG)	0.416	<0.454	ns	
4800C	14.166	14.166	34	tCK(AVG)	RESERVED		ns	
Supported CL					22,26,28,30,32,36,40,42		nCK	

NOTE :

1) Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.
2) The translation of all timing parameters from ns values to nCK values shall follow the Rounding Algorithm. The translation of tAA to CL shall follow the explicit combinations listed in the Speed Bin Tables.
3) The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When selecting tCK(avg), requirements from the CL setting as well as requirements from the CWL setting shall be fulfilled.
4) 'Reserved' settings are not allowed. The user shall program a different value.
5. This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm, depending on the specific speed bin and down clock frequency combination.
6) DDR5-3200 AC timings apply if the DRAM operates slower than the 2933 MT/s data rate. This is not limited to only the Speed Bin Table timings.
7) Parameters apply from tCK(avg)min to tCK(avg)max.
8) tRC(min) shall always be greater than or equal to tRAS(min) + tRP(min), and when using the appropriate rounding algorithms, nRC(min) shall always be greater than or equal to nRAS(min) + nRP(min).
9) tCK(avg).max of 1.010 ns (1980 MT/s data rate) is defined to allow for 1% SSC down-spreading at a data rate of 2000 MT/s according to JESD404-1.
10) Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC standard. The JEDEC standard does not require support for all speed bins within a given speed. The JEDEC standard requires meeting the parameters for a least one of the listed speed bins.
11) Any speed bin also supports functional operation at slower frequencies as shown in the table which are not subject to Production Tests but are verified by Design/Characterization.
12) The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the Speed Bin Tables. The CL Algorithm calculates supported CAS Latencies by rounding the operating frequency up to the next faster native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting tCK(AVG)min, and the bin target timings, the CL Algorithm then uses the Rounding Algorithm to calculate the valid CAS Latency. Because the DDR5 SDRAM specification only supports even CAS Latencies, odd CAS Latencies are rounded up to the next even CAS Latency. The 1980-2100 MT/s data rate always uses CL22. If tAA(corrected) or tRCDtRP(corrected) are violated, the CL Algorithm uses a slower combination of tAA(target) and tRCDtRP(target) to return slower valid CAS Latencies. The DDR5 SDRAM can support up to four valid CAS Latencies, CL(AN), CL(B), CL(BN), and CL(C), for a given frequency. tAA(corrected) and tRCDtRP(corrected) are calculated by reducing tAA(min), tRCD(min), and tRP(min) by the Rounding Algorithm correction factor. The proper setting of CL shall be determined by the memory controller, either by using the Speed Bin Tables, or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information.

13.0 IDD,IDDQ,IPP SPECIFICATION PARAMETERS AND TEST CONDITIONS

13.1 IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 226 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDDQ0, IPP0, IDD0F, IDDQ0F, IPP0F, IDD2N, IDDQ2N, IPP2N, IDD2NT, IDDQ2NT, IPP2NT, IDD2P, IDDQ2P, IPP2P, IDD3N, IDDQ3N, IPP3N, IDD3P, IDDQ3P, IPP3P, IDD4R, IDDQ4R, IPP4R, IDD4RC, IDD4W, IDDQ4W, IPP4W, IDD4WC, IDD5F, IDDQ5F, IPP5F, IDD5B, IDDQ5B, IPP5B, IDD5C, IDDQ5C, IPP5C, IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD7, IDDQ7, IPP7, IDD8, IDDQ8, IPP8 and IDD9, IDDQ9, IPP9) are measured as time-averaged currents with all VDD balls of the DDR5 SDRAM under test tied together. Any IDDQ or IPP current is not included in IDD currents.
- IDDQ currents are measured as time-averaged currents with all VDDQ balls of the DDR5 SDRAM under test tied together. Any IDD or IPP current is not included in IDDQ currents.
- IPP currents are measured as time-averaged currents with all VPP balls of the DDR5 SDRAM under test tied together. Any IDD or IDDQ current is not included in IPP currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR5 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 38.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as VIN <= VILAC(max).
- "1" and "HIGH" is defined as VIN >= VIHAC(min).
- "MID-LEVEL" is defined as inputs are VREF = 0.75 * VDDQ.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 272.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Chapter 11.2 through Chapter 11.11.
- IDD Measurements are done after properly initializing and training the DDR5 SDRAM. This includes but is not limited to setting
  TDQS_t disabled in MR5;
  CRC disabled in MR50;
  DM disabled in MR5;
  1N mode enabled and set CS assertion duration (MR2:OP[4]) as 1B in MR2, unless otherwise specified in the IDD, IDDQ and IPP patterns' conditions definitions;
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD, IDDQ or IPP measurement is started, with the exception of IDD9 which can be measured any time after the DRAM has entered MBIST mode.
- T_{CASE} defined as 0 - 95°C, unless stated in the specific condition definition table below.
- For all IDD, IDDQ and IPP measurement loop timing parameters, refer to the timing parameters defined in the spec to calculate the nCK required.

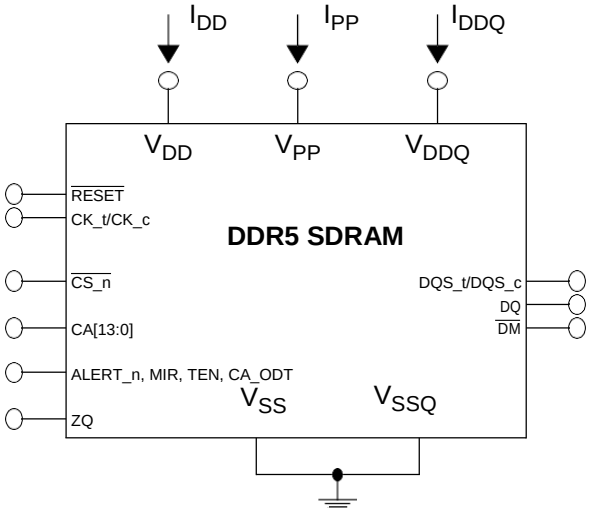


Figure 37. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

NOTE :
1) DIMM level Output test load condition may be different from above.

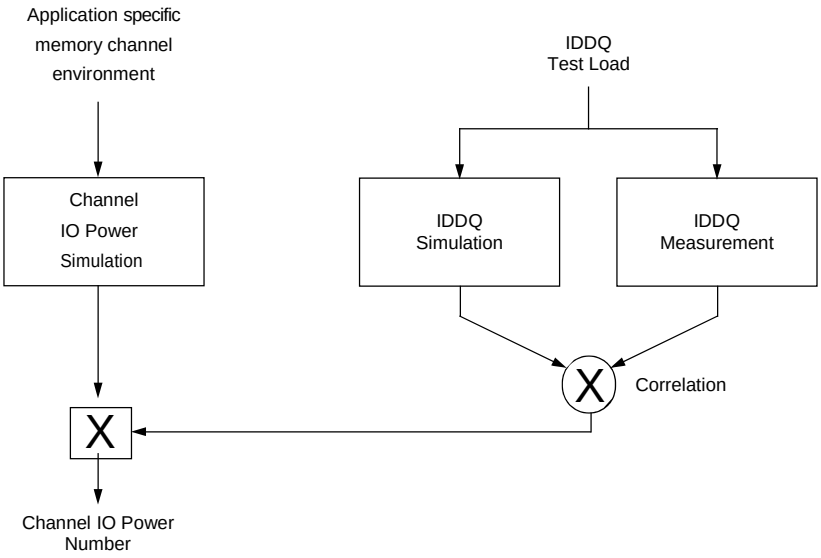


Figure 38. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

[Table 48] Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** **External clock:** On; **BL:** 161; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to Table 49; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 49); **Output Buffer and RTT:** Enabled in Mode Registers2; **Pattern Details:** see Table 49
IDDQ0	**Operating One Bank Active-Precharge IDDQ Current** **Same condition with IDD0,** however measuring IDDQ current instead of IDD current
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0,** however measuring IPP current instead of IDD current
IDD0F	**Operating Four Bank Active-Precharge Current** **External clock:** On; **BL:** 161; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to Table 50; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with four bank active at a time: (see Table 50); **Output Buffer and RTT:** Enabled in Mode Registers2; **Pattern Details:** see Table 50
IDDQ0F	**Operating Four Bank Active-Precharge IDDQ Current** **Same condition with IDD0F,** however measuring IDDQ current instead of IDD current
IPP0F	**Operating Four Bank Active-Precharge IPP Current** **Same condition with IDD0F,** however measuring IPP current instead of IDD current
IDD2N	**Precharge Standby Current** **External clock:** On; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to Table 51; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers2; Pattern Details: see Table 51
IDDQ2N	**Precharge Standby IDDQ Current** **Same condition with IDD2N,** however measuring IDDQ current instead of IDD current
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N,** however measuring IPP current instead of IDD current
IDD2NT	**Precharge Standby Non-Target Command Current** **External clock:** On; **BL:** 161; **CS_n:** High between WRITE commands; **CS_n, CA Inputs:** partially toggling according to Table 52; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; Pattern Details: see Table 52
IDDQ2NT (Optional)	**Precharge Standby Non-Target Command IDDQ Current** **Same condition with IDD2NT, however measuring IDDQ current instead of IDD current**
IPPQ2NT (Optional)	**Precharge Standby Non-Target Command IPP Current** **Same condition with IDD2NT, however measuring IPP current instead of IDD current**
IDD2P	**Precharge Power-Down** **Device in Precharge Power-Down, External clock:** On; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank** Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2;
IDDQ2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IDDQ current instead of IDD current
IPP2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IPP current instead of IDD current
IDD3N	**Active Standby Current** **External clock:** On; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to Table 51; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers2; Pattern Details: see Table 51
IDDQ3N	**Active Standby IDDQ Current** **Same condition with IDD3N,** however measuring IDDQ current instead of IDD current
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N,** however measuring IPP current instead of IDD current
IDD3P	**Active Power-Down Current** **Device in Active Power-Down, External clock:** On; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank** Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2;
IDDQ3P	**Active Power-Down IDDQ Current** **Same condition with IDD3P,** however measuring IDDQ current instead of IDD current

[Table 48] Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P,** however measuring IPP current instead of IDD current
IDD4R	**Operating Burst Read Current** **External clock:** On; **BL:** 161; **CS_n:** High between RD; **CA Inputs:** partially toggling according to Table 53; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 53; **DM_n:** stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 53); **Output Buffer and RTT:** Enabled in Mode Registers2; Pattern Details: see Table 53
IDD4RC	**Operating Burst Read Current with Read CRC** **Read CRC enabled4. Other conditions:** see IDD4R
IDDQ4R	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R,** however measuring IPP current instead of IDD current
IDD4W	**Operating Burst Write Current** **External clock:** On; **BL:** 161; **CS_n:** High between WR; **CA Inputs:** partially toggling according to Table 54; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 54; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 54; **Output Buffer and RTT:** Enabled in Mode Registers2; Pattern Details: see Table 54
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled3, Other conditions:** see IDD4W
IDDQ4W	**Operating Burst Write IDDQ Current** **Same condition with IDD4W,** however measuring IDDQ current instead of IDD current
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W,** however measuring IPP current instead of IDD current
IDD5B	**Burst Refresh Current (Normal Refresh Mode)** **External clock:** On; **BL:** 161; **CS_n**: High between REF; **CA Inputs:** partially toggling according to Table 55; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC1 (see Table 55); **Output Buffer and RTT:** Enabled in Mode Registers2; **Pattern Details:** see Table 55
IDDQ5B	**Burst Refresh IDDQ Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IDDQ current instead of IDD current
IPP5B	**Burst Refresh IPP Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IPP current instead of IDD current
IDD5F	**Burst Refresh Current (Fine Granularity Refresh Mode)** **tRFC=tRFC2, Other conditions:** see IDD5B
IDDQ5F	**Burst Refresh IDDQPP Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IDDQ current instead of IDD current
IPP5F	**Burst Refresh IPP Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IPP current instead of IDD current
IDD5C	**Burst Refresh Current (Same Bank Refresh Mode)** **External clock:** On; **tCK, nRFCsb**: see Table 56; **BL:** 161; **CS_n**: High between REF; **CAInputs:** partially toggling according to Table 56; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFCsb (see Table 56); **Output Buffer and RTT:** Enabled in Mode Registers2; Pattern Details: see Table 56
IDDQ5C	**Burst Refresh IDDQPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IDDQ current instead of IDD current
IPP5C	**Burst Refresh IPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IPP current instead of IDD current
IDD6N	**Self Refresh Current: Normal Temperature Range** ***T*CASE:** 0 - 85°C; **External clock:** Off; CK_t and CK_c#: HIGH; **BL:** 161; **CS_n#:** low; **CA, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers2;
IDDQ6N	**Self Refresh IDDQ Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IDDQ current instead of IDD current
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IPP current instead of IDD current

[Table 48] Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IDD6E	**SelfRefresh Current: Extended Temperature Range**) ***T*CASE:** 85 - 95°C; Extended4; **External clock:** Off; CK_t and CK_c: HIGH; **BL:** 161; **CS_n:** low; **CA, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers2
IDDQ6E	**Self Refresh IDDQ Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IDDQ current instead of IDD current
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IPP current instead of IDD current
IDD7	**Operating Bank Interleave Read Current** **External clock:** On; **BL:** 161; **CS_n**: High between ACT and RDA; **CA Inputs:** partially toggling according to Table 58; **Data IO:** read data bursts with different data between one burst and the next one according to Table 58; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 58; **Output Buffer and RTT:** Enabled in Mode Registers2; Pattern Details: see Table 58
IDDQ7	**Operating Bank Interleave Read IDDQ Current** **Same condition with IDD7,** however measuring IDDQ current instead of IDD current
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7,** however measuring IPP current instead of IDD current
IDD8	**Maximum Power Saving Deep Power Down Current** **External clock:** Off; CK_t and CK_c#: HIGH; **BL:** 161; **CS_n#:** low; **CA:**High**, DM_n:** stable at 1; **Bank Activity:** All banks closed and device in MPSM deep power down mode5; **Output Buffer and RTT:** Enabled in Mode Registers2; Patterns Details: same as IDD6N but MPSM is enabled in mode register.
IDDQ8	**Maximum Power Saving Deep Power Down IDDQ Current** **Same condition with IDD8,** however measuring IDDQ current instead of IDD current
IPP8	**Maximum Power Saving Deep Power Down IPP Current** **Same condition with IDD8,** however measuring IPP current instead of IDD current

NOTE :

1) Burst Length: BL16 fixed by MR0 OP[1:0]=00
2) Output Buffer Enable
- set MR5 OP[0] = 0] : Qoff = Output buffer enabled
- set MR5 OP[2:1] = 00]: Pull-Up Output Driver Impedance Control = RZQ/7
- set MR5 OP[7:6] = 00]: Pull-Down Output Driver Impedance Control = RZQ/7
RTT_Nom enable
- set MR35 OP[5:0] = 110110: RTT_NOM_WR = RTT_NOM_RD = RZQ/6
RTT_WR enable
- set MR34 OP[5:3] = 010 RTT_WR = RZQ/2
RTT_PARK disable
- set MR34 OP[2:0] = 000
3) WRITE CRC enabled
- set MR50 OP[2:1] = 11
4) Read CRC enabled
- set MR50:OP[0]=1
5) MPSM Deep Power Down Mode
- set MR2:OP[3]=1 if PDA Enumerate ID not equal to 15
- set MR2:OP[5]=1 if PDA Enumerate ID equal to 15

13.2 IDD0, IDDQ0, IPP0 Pattern

Executes Active and PreCharge commands with tightest timing possible while exercising all Bank and Bank Group addresses. Note 2 applies to the entire table.

[Table 49] IDD0, IDDQ0, IPP0

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H	-	0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling					Repeat sequence to satisfy tRAS(min), truncate if required
	2	PREpb	L	-		0x0	0x00	0x0	
	3	DES	H	Toggling					Repeat sequence to satisfy tPR(min), truncate if required
	4	ACT	L H	-	0x03FFF	0x0	0x00	0x0	
	5	DES	H	Toggling					Repeat sequence to satisfy tRAS(min), truncate if required
	6	PREpb	L	-		0x0	0x00	0x0	
	7	DES	H	Toggling					Repeat sequence to satisfy tPR(min), truncate if required
1	8-15	Repeat sub-loop 0, use BG[2:0]=0x1 instead							
2	16-23	Repeat sub-loop 0, use BG[2:0]=0x2 instead							
3	24-31	Repeat sub-loop 0, use BG[2:0]=0x3 instead							
4	32-39	Repeat sub-loop 0, use BG[2:0]=0x4 instead							skip for x16
5	40-47	Repeat sub-loop 0, use BG[2:0]=0x5 instead							skip for x16
6	48-55	Repeat sub-loop 0, use BG[2:0]=0x6 instead							skip for x16
7	56-63	Repeat sub-loop 0, use BG[2:0]=0x7 instead							skip for x16
8-15	64-127	Repeat sub loops 0-7, use BA[1:0]=0x1 instead							
16-23	128-191	Repeat sub loops 0-7, use BA[1:0]=0x2 instead							
24-31	192-255	Repeat sub loops 0-7, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-31 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

NOTE :
1) Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.

13.3 IDD0F, IDDQ0F, IPP0F Pattern

Executes a rolling four bank group Active and PreCharge commands per tRC time while exercising all Bank, Bank, Group and CID addresses. Note 2 applies to the entire table.

[Table 50] IDD0F, IDDQ0F, IPP0F

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H		0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	2	ACT	L H		0x00000	0x0	0x01	0x0	
	3	DES	H	Toggling					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	4	ACT	L H		0x00000	0x0	0x02	0x0	
	5	DES	H	Toggling					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	6	ACT	L H		0x00000	0x0	0x03	0x0	
	7	DES	H	Toggling					Repeat to satisfy tRAS(min) from Sequence 0
	8	PREpb	L			0x0	0x00	0x0	
	9	DES	H	Toggling					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	10	PREpb	L			0x0	0x01	0x0	
	11	DES	H	Toggling					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	12	PREpb	L			0x0	0x02	0x0	
	13	DES	H	Toggling					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	14	PREpb	L			0x0	0x03	0x0	
	15	DES	H	Toggling					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	16	DES	H	Toggling					Repeat for tRC(min) from Sequence 0 first ACTIVATE. This will be zero DESELECTS for speed 4000Mbps and slower.
1	17-33	Repeat sub-loop 0, use Row Address = 0x03FFF for the ACT instead							
2-3	34-67	Repeat sub-loop 0-1, use BG[2:0]=0x4,0x5,0x6,0x7 instead of 0x0,0x1,0x2,0x3							skip for x16
4-7	68-101	Repeat sub-loops 0-3, use BA[1:0]=0x1 instead							
8-11	102-135	Repeat sub-loops 0-3, use BA[1:0]=0x2 instead							
12-15	136-169	Repeat sub-loops 0-3, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-15 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

NOTE :
1) Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.

13.4 IDD2N, IDD3N Pattern

Executes DESELECT commands while exercising all command/address pins in a predefined pattern. All notes apply to entire table.

[Table 51] IDD2N, IDDQ2N, IPP2N, IDD3N, IDDQ3N, IPP3N

Sequence	Command	CS	C/A [13:0]
0	DES	H	0x0000
1	DES	H	0x3FFF
2	DES	H	0x3FFF
3	DES	H	0x3FFF

NOTE :
1) Data is pulled to VDDQ
2) DQS_t and DQS_c are pulled to VDDQ
3) Command / Address ODT is disabled
4) Repeat sequence 0 through 3
5) All banks of all logical ranks mimic the same test condition

13.5 IDD2NT, IDDQ2NT, IPP2NT Pattern

Executes Non-Target WRITE commands simulating Rank to Rank timing while exercising all C/A bits. Notes 3-6 apply to entire table.

[Table 52] IDD2NT, IDDQ2NT, IPP2NT

Sequence	Command	CS_n	C/A [13:0]	Special Instructions
0	WRITE	L	0x002D	All valid C/A inputs to VSS
		L	0x0000	
1	DES	H	Toggling	Repeat sequence to meet 1*tCCD_S(min), truncate if required
2	WRITE	L	0x3FED	All valid C/A inputs to VDDQ
		L	0x3FFF	
3	DES	H	Toggling	Repeat sequence to meet 1*tCCD(min), truncate if required

NOTE :
1) WRITE with CS_n=L on both cycles indicated a non-target WRITE
2) Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern
3) Time between Non-Target WRITEs reflect tCCD_S (min) for one rank
4) DQ signals are VDDQ
5) DQS_t, DQS_c are VDDQ
6) Repeat 0 through 3

13.6 IDD4R, IDDQ4R, IPP4R Pattern

Executes READ commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-9 apply to entire table

[Table 53] IDD4R, IDDQ4R, IPP4R

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	READ	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	READ	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	READ	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling						Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	READ	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling						Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

NOTE :

1) Utilize DESELECTs between commands while toggling all C/A bits 100% each cycle (0x3FFF, 0x0000, 0x3FFF, 0x0000...) per the 4-cycle sequence defined in the IDD2N, IDD3N pattern
2) READs performed with Auto Precharge = H, Burst Chop = H
3) Row address is set to 0x0000
4) Data reflects burst length of 16
5) Data Pattern A for x4: 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0x0, 0xF
6) Data Pattern B for x4: 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0xF, 0x0
7) Data Pattern for x8 each beat will reflect two like nibbles (Data Pattern A = 0x00, 0xFF, 0xFF...)
8) Data Pattern for x16 each beat will reflect two like bytes (Data Pattern A = 0x0000, 0xFFFF, 0xFFFF...)
9) Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state

13.7 IDD4W, IDDQ4W, IPP4W Pattern

Executes WRITE commands with tightest timing possible while exercising all Bank, Bank Group and CDI CID addresses. Notes 2-6 apply to entire table.

[Table 54] IDD4W, IDDQ4W, IPP4W

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	WRITE	L	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	WRITE	L	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 i nstead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	WRITE	L	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	WRITE	L	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

NOTE :
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern
2) WRITEs performed with Auto Precharge = H, Burst Chop = TBD
3) Row address is set to 0x0000
4) Data reflects burst length of 16
5) Refer to IDD4R measurement loop table for data pattern definition
6) Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state

13.8 IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F Pattern

Executes Refresh (all Banks) command at minimum tRFC. Notes 3-6 apply to entire table.

[Table 55] IDD5B, IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F

Sub-Loop	Command	CS	C/A [13:0]	CA8	CID[2:0]	Special Instructions
0	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
1	DES	H	Toggling	-	-	Repeat sequence to satisfy tRFC(min), truncate if required
2	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
3	DES	H	Toggling	-	-	Repeat sequence to satisfy tRFC(min), truncate if required
...	Repeat sequence 0-3 for each 3DS logical rank, if applicable					CID[2:0]=0x1-0x7

NOTE :
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern
2) For IDD5B, use tRFC1(min). For IDD5F, use tRFC2(min)
3) DQ signals are VDDQ
4) All banks of all “non-target” logical ranks are Idd2N condition
5) Where C/A[13:0] column is not populated, refer to command truth table, CA8, and CID columns for the C/A state
6) Must set CA8=H on REFab commands to indicate 1X refresh rate on devices that support RIR

13.9 IDD5C, IDDQ5C and IPP5C Patterns

Executes Refresh (Same Bank) command at minimum tRFCsb. Notes 2-5 apply to entire table.

[Table 56] IDD5C, IDDQ5C, IPP5C

Sub-Loop	Command	CS	C/A [13:0]	CA8	BA[1:0]	CID[2:0]	Special Instructions
0	REFsb	L	-	H	0x0	0x0	
1	DES	H	Toggling	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
2	REFsb	L	-	H	0x1	0x0	
3	DES	H	Toggling	-		-	Repeat sequence to satisfy tRFCsb(min), truncate if required
4	REFsb	L	-	H	0x2	0x0	
5	DES	H	Toggling	-		-	Repeat sequence to satisfy tRFCsb(min), truncate if required
6	REFsb	L	-	H	0x3	0x0	
7	DES	H	Toggling	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
...	Repeat sequence 0-7 for each 3DS logical rank, if applicable						CID[2:0]=0x1-0x7

NOTE :
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern
2) DQ signals are VDDQ
3) All banks of all “non-target” logical ranks are Idd2N condition
4) Where C/A[13:0] column is not populated, refer to command truth table, CA8, and CID columns for the C/A state
5) All banks of all “non-target” logical ranks are Idd2N condition

13.10 IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R Pattern

All notes apply to entire table.

[Table 57] IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R

Sub-Loop	Command	Clock	CS	C/A[13:0]	Special Instructions
0	SRE	Valid	L	0x3BF7	Clocks must be valid tCKLCS(min) time
1	DES	Valid	H	0x3FFF	Repeat sequence to satisfy tCPDED(min), truncate if required
2	All C/A=H	Valid	L	0x3FFF	
3	All C/A=H	CK_t = CK_c = H	L	0x3FFF	Repeat sequence indefinitely

NOTE :
1) Data is pulled to VDDQ
2) DQS_t and DQS_c are pulled to VDDQ
3) ODT disabled in Mode Registers

13.11 IDD7, IDDQ7 and IPP7 Patterns

Executes ACTVATE, READ/A commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-6 apply to entire table.

[Table 58] IDD7, IDD7Q, IPP7

Sub-Loop	Sequence	Com-mand	CS	C/A[13:0]	Row Address [17:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	ACT	L H	-	0x00000	-	0x0	0x0	0x0	-	
	1	DES	H	Toggling							Repeat sequence to satisfy tRRD_S(min)
1	2	ACT	L H	-	0x03FFF	-	0x1	0x1	0x0	-	
	3	DES	H	Toggling							Repeat sequence to satisfy tRRD_S(min)
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead									
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead									
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead									skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead									skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead									skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead									skip for x16
8	16	RDA	L H	-	-	0x3F0	0x0	0x0	0x0	Pattern A	
	17	ACT	L H	-	0x00000	-	0x1	0x0	0x0	-	
	18	DES	H	Toggling							Repeat sequence to satisfy tCCD_S(min)
9	19	RDA	L H	-	-	0x000	0x0	0x0	0x0	Pattern B	
	20	ACT	L H	-	0x03FFF	-	0x1	0x1	0x0	-	
	21	DES	H	Toggling							Repeat sequence to satisfy tCCD_S(min)
10	22-24	Repeat sub-loop 8, use BG[2:0]=0x2 instead									
11	25-27	Repeat sub-loop 9, use BG[2:0]=0x3 instead									
12	28-30	Repeat sub-loop 8, use BG[2:0]=0x4 instead									skip for x16
13	31-33	Repeat sub-loop 8, use BG[2:0]=0x5 instead									skip for x16
14	34-36	Repeat sub-loop 8, use BG[2:0]=0x6 instead									skip for x16
15	37-39	Repeat sub-loop 8, use BG[2:0]=0x7 instead									skip for x16
16-23	40-64	Repeat sub-loops 8-15, use BA[1:0]=0x1 for the RDA and BA[1:0]=0x2 for the ACT									
24-31	65-89	Repeat sub-loops 8-15, use BA[1:0]=0x2 for the RDA and BA[1:0]=0x3 for the ACT									
32-39	90-114	Repeat sub-loops 8-15, use BA[1:0]=0x3 for the RDA and BA[1:0]=0x0 for the ACT									
...	...	Repeat sub-loops 0-18 for each 3DS logical rank, if applicable									CID[2:0]=0x1-0x7

NOTE :
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern
2) READs performed with Auto Precharge = H, Burst Chop = H
3) x8 or x16 may have different Bank or Bank Group Address
4) Data reflects burst length of 16
5) Refer to IDD4R measurement loop table for data pattern definition

14.0 IDD SPEC TABLE

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

Symbol	M321R2GA3BB0: 1Rx8 16GB Module			Unit
	DDR5-4800			
	40-39-39			
	IDD Max.	IDDQ Max.	IPP Max.	
	VDD 1.1V		VPP 1.8V	
I_{DD0}	442	867	70	mA
I_{DD0F}	838	867	120	mA
I_{DD2N}	177	866	40	mA
I_{DD2P}	93	374	40	mA
I_{DD2NT}	545	875	40	mA
I_{DD3N}	288	867	50	mA
I_{DD3P}	158	611	50	mA
I_{DD4R}	1742	2186	80	mA
I_{DD4RC}	1742	2186	80	mA
I_{DD4W}	2213	2503	70	mA
I_{DD4WC}	2213	2503	70	mA
I_{DD5B}	1663	965	570	mA
I_{DD5F}	1617	965	560	mA
I_{DD5C}	666	965	240	mA
I_{DD6N}	363	285	100	mA
I_{DD7}	3220	2186	290	mA
I_{DD8}	83	290	30	mA

Symbol	M321R4GA3BB0: 2Rx8 32GB Module			Unit
	DDR5-4800			
	40-39-39			
	IDD Max.	IDDQ Max.	IPP Max.	
	VDD 1.1V		VPP 1.8V	
I_{DD0}	617	1043	110	mA
I_{DD0F}	1002	1032	160	mA
I_{DD2N}	399	1043	80	mA
I_{DD2P}	282	550	80	mA
I_{DD2NT}	717	1041	80	mA
I_{DD3N}	665	1199	100	mA
I_{DD3P}	595	985	100	mA
I_{DD4R}	2109	2362	120	mA
I_{DD4RC}	2109	2362	120	mA
I_{DD4W}	2573	2679	110	mA
I_{DD4WC}	2573	2679	110	mA
I_{DD5B}	1901	1141	610	mA
I_{DD5F}	1815	1120	600	mA
I_{DD5C}	1232	1397	280	mA
I_{DD6N}	526	441	200	mA
I_{DD7}	3372	2338	330	mA
I_{DD8}	235	442	60	mA

Symbol	M321R4GA0BB0: 1Rx4 32GB Module			Unit
	DDR5-4800			
	40-39-39			
	IDD Max.	IDDQ Max.	IPP Max.	
	VDD 1.1V		VPP 1.8V	
I_{DD0}	861	1051	140	mA
I_{DD0F}	1648	1060	260	mA
I_{DD2N}	370	1050	80	mA
I_{DD2P}	212	489	80	mA
I_{DD2NT}	1111	1059	80	mA
I_{DD3N}	638	1051	100	mA
I_{DD3P}	370	726	100	mA
I_{DD4R}	3120	2950	160	mA
I_{DD4RC}	3120	2950	160	mA
I_{DD4W}	5028	2802	160	mA
I_{DD4WC}	5028	2802	160	mA
I_{DD5B}	3370	1149	600	mA
I_{DD5F}	3278	1149	560	mA
I_{DD5C}	1351	1149	500	mA
I_{DD6N}	833	308	200	mA
I_{DD7}	6009	2946	600	mA
I_{DD8}	157	317	60	mA

Symbol	M321R8GA0BB0: 2Rx4 64GB Module			Unit
	DDR5-4800			
	40-39-39			
	IDD Max.	IDDQ Max.	IPP Max.	
	VDD 1.1V		VPP 1.8V	
I_{DD0}	1229	1322	220	mA
I_{DD0F}	2016	1330	340	mA
I_{DD2N}	738	1322	160	mA
I_{DD2P}	424	650	160	mA
I_{DD2NT}	2215	1347	160	mA
I_{DD3N}	1273	1322	200	mA
I_{DD3P}	738	891	200	mA
I_{DD4R}	3036	2989	240	mA
I_{DD4RC}	3036	2989	240	mA
I_{DD4W}	4696	2860	240	mA
I_{DD4WC}	4696	2860	240	mA
I_{DD5B}	3253	1420	680	mA
I_{DD5F}	3173	1420	640	mA
I_{DD5C}	1496	1420	580	mA
I_{DD6N}	1445	344	400	mA
I_{DD7}	5550	2987	680	mA
I_{DD8}	273	360	120	mA

[Table 59] DIMM Operating Status

IDD Status	Operating Rank	The other Rank
I_{DD0}	I_{DD0}	I_{DD2N}
I_{DD2P}	I_{DD2P}	I_{DD2P}
I_{DD2N}	I_{DD2N}	I_{DD2N}
I_{DD3P}	I_{DD3P}	I_{DD3P}
I_{DD3N}	I_{DD3N}	I_{DD3N}
I_{DD4R}	I_{DD4R}	I_{DD2N}
I_{DD4W}	I_{DD4W}	I_{DD2N}
I_{DD5B}	I_{DD5B}	I_{DD2N}
I_{DD6}	I_{DD6}	I_{DD6}
I_{DD7}	I_{DD7}	I_{DD2N}
I_{DD8}	I_{DD8}	I_{DD8}

15.0 INPUT/OUTPUT CAPACITANCE

[Table 60] Silicon Pad I/O Capacitance

Symbol	Parameter	DDR5-4400		DDR5-4800		Unit	NOTE
		min	max	min	max		
C_{IO}	Input/output capacitance (DQ, DM_n, DQS_t, DQS_c, TDQS_t, TDQS_c)	0.45	0.9	0.45	0.9	pF	1,2
C_{DIO}	Input/output capacitance delta (DQ, DM_c)	-0.1	0.1	-0.1	0.1	pF	1,2,8
C_{DDQS}	Input/output capacitance delta (DQS_t and DQS_c)		0.04		0.04	pF	1,2,4
C_{CK}	Input capacitance (CK_t and CK_c)	0.2	0.6	0.2	0.6	pF	1,2
C_{DCK}	Input capacitance delta (CK_t and CK_c)		0.05		0.05	pF	1,2,3
C_I	Input capacitance (CS_n & CA[13:0] pins only)	0.2	0.6	0.2	0.6	pF	1,2,5
$C_{DI\_CS\_n}$	Input capacitance delta (CS_n pin only)	-0.1	0.1	-0.1	0.1	pF	1,2,6
C_{DI_CA}	Input capacitance delta (CA[13:0] pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,7
C_{ALERT}	Input/output capacitance of ALERT	0.4	1.5	0.4	1.5	pF	1,2
$C_{Loopback}$	Input/output capacitance of Loopback (LBDQ, LBDQS)	0.3	1.0	0.3	1.0	pF	1,2
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,2,9
C_{ZQ}	Input capacitance of ZQ	-	5	-	5	pF	1,2,11
C_{STRAP}	Input capacitance of MIR, CAI, CA_ODT pins	-	10	-	10	pF	1,2,10

NOTE :

1) This parameter is not subject to production test. This parameter is measured by using vendor specific measurement methodology.
2) This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
3) Absolute value CIO(CK_t)-CIO(CK_c)
4) Absolute value of CIO(DQS_t)-CIO(DQS_c)
5) CI applies to CS_n and CA[13:0]
6) CDI_CS_n = CI(CS_n)-0.5*(CI(CK_t)+CI(CK_c))
7) CDI_CA =CI(CA[13:0])-0.5*(CI(CK_t)+CI(CK_c))
8) CDIO = CIO(DQ,DM)-Avg(CIO(DQ,DM))
9) TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.
10) MIR, CAI, and CA_ODT are strap pins used to configure module or point to point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.
11) Maximum external load capacitance on ZQ pin: 25pF. The ZQ functionality / accuracy with the max capacitive load is characterized.

16.0 tREFI and tRFC Parameters

The maximum average refresh interval (tREFI) requirement for the DDR5 SDRAM depends on the refresh mode setting (Normal or FGR), and the device's case temperature (Tcase). When the refresh mode is set to Normal Refresh mode, REFab commands are issued (tRFC1), and Tcase<=85°C, the maximum average refresh interval (tREFI1) is tREFI. When the refresh mode is set to FGR mode, REFab commands are issued (tRFC2) and Tcase<=85°C, the maximum average refresh interval (tREFI2) is tREFI/2. This same tREFI/2 interval value is also appropriate if the refresh mode is set to Normal Refresh mode and REFab commands are issued (tRFC1) but 85°C<Tcase<=95°C. Finally, if the refresh mode is set to FGR mode, REFab commands are issued (tRFC2), and 85°C<Tcase<=95°C, the maximum average refresh interval (tREFI2) is tREFI/4.

The DDR5 SDRAM includes an optional method for the host to indicate when Refresh commands are being issued at the 2x (tREFI2) refresh interval rate. The 2x Refresh Interval Rate indicator (MR4:OP[3]) alerts the DRAM if the host supports the refresh interval rate indication as part of the REF command using CA8. If enabled (MR4:OP[3]=1), the host will issue 1x REF commands with CA8=H (Tcase<=85°C), and the host will issue 2x REF commands with CA8=L (Tcase any allowable temperature). MR4:OP[3] is a Status Read/Write "SR/W" MR bit which shows DDR5 SDRAM support of this optional feature. Reading MR4:OP[3] will return a "1" if the 2x Refresh Interval Rate indicator is supported. A "0" will be returned if not supported.
tREFI is based on the 8,192 refresh commands that need to be issued within the baseline tREF=32ms refresh period on the DDR5 SDRAM.

[Table 61] tREFI parameters for REFab and REFsb Commands

Command	Refresh Mode	Symbol & Range		Expression	Value	Unit	Notes
REFab	Normal	tREFI1	0ºC <= TCASE <= 85ºC	tREFI	3.9	us	
			85ºC < TCASE <= 95ºC	tREFI/2	1.95	us	
REFab	Fine Granularity	tREFI2	0ºC <= TCASE <= 85ºC	tREFI/2	1.95	us	
			85ºC < TCASE <= 95ºC	tREFI/4	0.975	us	
REFsb	Fine Granularity	tREFIsb	0ºC <= TCASE <= 85ºC	tREFI/(2*n)	1.95/n	us	1
			85ºC < TCASE <= 95ºC	tREFI/(4*n)	0.975/n	us	1

NOTE :
1) *n* is the number of banks in a bank group (e.g. 8G: n=2; 16G: n=4).

[Table 62] tRFC parameters by device density

Refresh Mode	Symbol	16Gb	Unit	Notes
Normal Refresh (REFab)	tRFC1(min)	295	ns	
Fine Granularity Refresh (REFab)	tRFC2(min)	160	ns	
Same Bank Refresh (REFsb)	tRFCsb(min)	130	ns	

[Table 63] Same Bank Refresh parameters

Refresh Mode	Symbol	16Gb	Unit	Notes
Same Bank Refresh to ACT delay SLR	tREFSBRD_slr(min)	30	ns	
Same Bank Refresh to ACT delay DLR	tREFSBRD_dlr(min)	15	ns	

17.0 TIMING PARAMETERS BY SPEED GRADE

17.1 Timing Parameters by Speed Bin for DDR5-4400

Speed		DDR5-4400		Units	NOTE
Parameter	Symbol	MIN	MAX		
Clock Timing					
Average Clock Period	tCK(avg)	0.454	-	ns	1
Command and Address Timing					
Read to Read command delay for same bank group	tCCD_L	max(8nCK,5ns)	-	nCK, ns	
Write to Write command delay for same bank group	tCCD_L_WR	max(32nCK, 20ns)	-	nCK, ns	
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)	-	nCK, ns	
Read to Write command delay for same bank group	tC-CD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK, ns	3,5,6
Write to Read command delay for same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)		nCK, ns	4,6
Read to Read command delay for different bank group	tCCD_S	8	-	nCK	
Write to Write command delay for different bank group	tCCD_S_WR	8	-	nCK	
Read to Write command delay for different bank group	tC-CD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK, ns	3,5,6
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)		nCK, ns	4,6
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP		nCK, ns	2,4,6
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	-	nCK, ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	-	nCK, ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	-	nCK	
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	nCK	
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 14.545ns)	-	nCK, ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 18.181ns)	-	nCK, ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	-	nCK, ns	
Precharge to Precharge command delay	tPPD	2	-	nCK	7
Write recovery time	tWR	30	-	ns	

17.0 Timing Parameters by Speed Bin for DDR5-4800

Speed		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX		
Clock Timing					
Average Clock Period	tCK(avg)	0.416	-	ns	1
Command and Address Timing					
Read to Read command delay for same bank group	tCCD_L	max(8nCK,5ns)	-	nCK, ns	
Write to Write command delay for same bank group	tCCD_L_WR	max(32nCK, 20ns)	-	nCK, ns	
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)	-	nCK, ns	
Read to Write command delay for same bank group	tC-CD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK, ns	3,5,6
Write to Read command delay for same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)		nCK, ns	4,6
Read to Read command delay for different bank group	tCCD_S	8	-	nCK	
Write to Write command delay for different bank group	tCCD_S_WR	8	-	nCK	
Read to Write command delay for different bank group	tC-CD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK, ns	3,5,6
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)		nCK, ns	4,6
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP		nCK, ns	2,4,6
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	-	nCK, ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	-	nCK, ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	-	nCK	
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	nCK	
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 13.333ns)	-	nCK, ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 16.666ns)	-	nCK, ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	-	nCK, ns	
Precharge to Precharge command delay	tPPD	2	-	nCK	7
Write recovery time	tWR	30	-	ns	

NOTE :

1) tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
2) tCCD_WTRA_slr(min) shall always be greater than or equal to CWL + WBL/2 + tWR_slr(min) - tRTP_slr(min), and when using the appropriate rounding algorithms, nCCD_WTRA_slr(min) shall always be greater than or equal to CWL + WBL/2 + nWR_slr(min) -nRTP_slr(min).
3) RBL : Read burst length associated with Read command.
   RBL = 32 for fixed BL32 and BL32 in BL32 OTF mode.
   RBL = 16 for fixed BL16 and BL16 in BL32 OTFmode.
   RBL = 16 for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode.
4) WBL: Write burst length associated with Write command.
   WBL = 32 for fixed BL32 and BL32 in BL32 OTF mode.
   WBL = 16 for fixed BL16 and BL16 in BL32 OTFmode.
   WBL = 16 for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode.
5) The following is considered for tRTW equation.
   1tCK needs to be added due to tDQS2CK.
   Read DQS offset timing can pull in the tRTW timing.
   1tCK needs to be added when 1.5tCK postamble.
6) CWL=CL-2.
7) tPPD applies to any combination of precharge commands.

17.1 DDR5 Function Matrix

DDR5 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

[Table 64] Function Matrix (By ORG. V:Supported, Blank:Not supported)

Functions	x4	x8	NOTE
Write Leveling	V	V	
Temperature controlled Refresh	V	V	
Fine Granularity Refresh	V	V	
Same Bank Refresh	V	V	
Refresh for Management			
Data Mask		V	
Command Address Inversion	V	V	
TDQS		V	
ZQ calibration	V	V	
DQ Vref Training	V	V	
Per DRAM Addressability	V	V	
Mode Register Readout	V	V	
WRITE CRC	V	V	
READ CRC	V	V	
Programmable Preamble/Postamble	V	V	
Maximum Power Saving Mode	V	V	
Connectivity Test Mode	V	V	
Bit Error Rate Test	V	V	
Package Output Driver Test Mode	V	V	
3DS	V		
CA Training Mode	V	V	
CS Training Mode	V	V	
DQS interval Oscillator	V	V	
ECC Transparency and Error Scrub	V	V	
Lookback	V	V	
Duty Cycle Adjuster	V	V	

18.0 DDR5 MODULE RANK AND CHANNEL TIMINGS

18.1 Module Rank and Channel Limitations for DDR5 DIMMs

To achieve efficient module power supply design for JEDEC-standard DDR5 DIMMs, minimum timings as well as limitations in the number of DRAMs are provided for Refresh, and Write operations occurring on a single module. As well, since these modules are organized as two independent 36-bit or 40-bit channels (32 bits for non-ECC DIMMs), additional restrictions apply in order to limit localized power delivery noise on the module. To provide best performance, the different channels may initiate commands on the same cycle provided the rank to rank timings are met, the maximum number of DRAMs in a given activity is not exceeded, and the applicable component timings shown elsewhere in this specification are met. The timing and operational relationships for DDR5 DIMMs are shown in Table 65 below.

[Table 65] DDR5 Module Rank and Channel Timings for DDR5 DIMMs

DIMM Configuration	Maximum number of DRAM die in simultaneous or overlapping activity			
	Refresh (All-Bank Refresh)		Write, Write-Pattern	
	Die per Physical Rank	Die per DIMM	Die per Channel	Die per DIMM
SR x16	No restriction			
DR x16	No restriction		2	4
SR x8	No restriction			
DR x8	No restriction		5	10
SR x4	No restriction			
DR x4	No restriction		10	20
Notes	1, 2, 3, 4, 7, 8, 9		1, 5, 6, 7, 9	

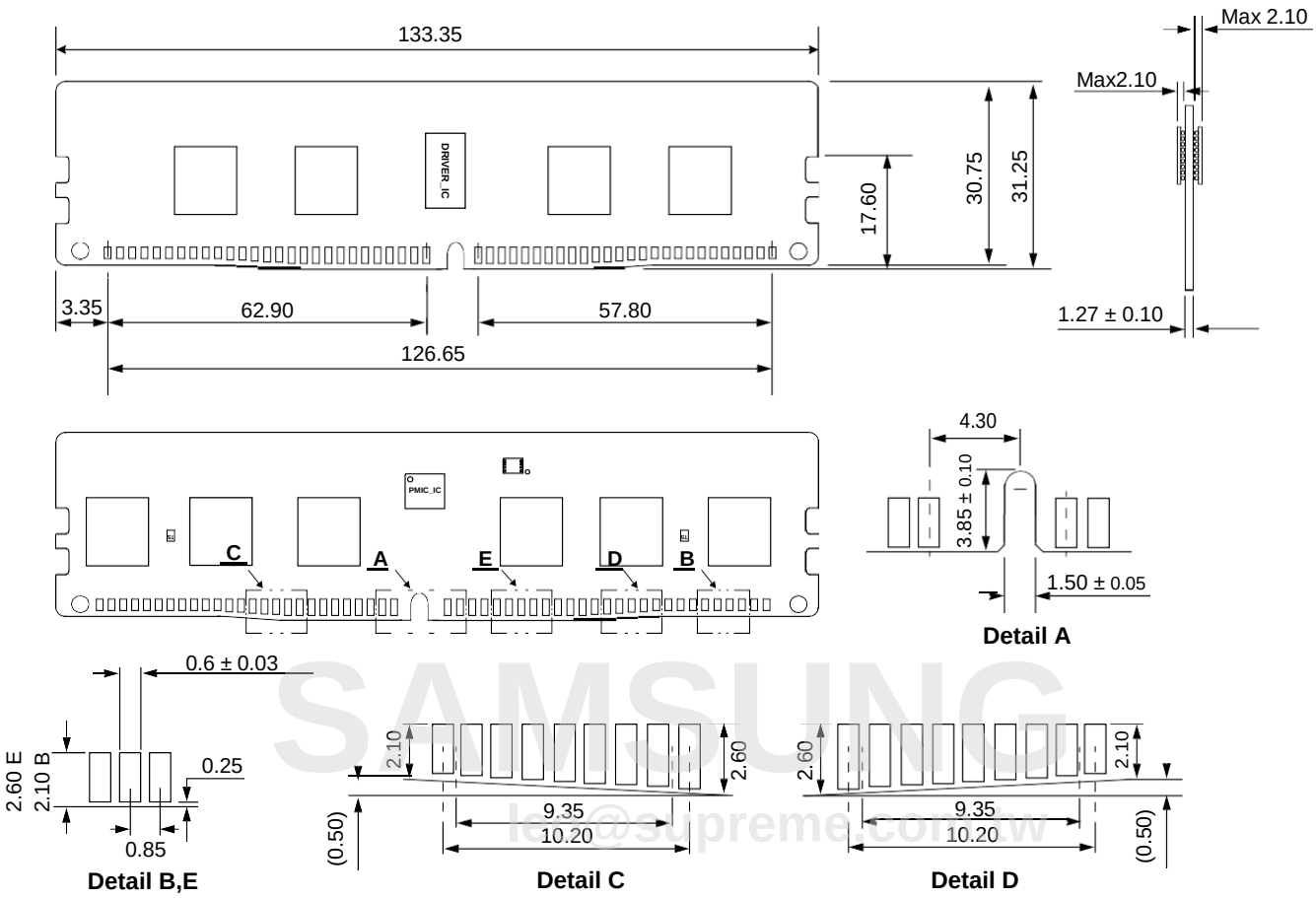
NOTE :

1) Any combination of commands with up to the maximum of die per channel and per DIMM, per condition is allowed
2) Refresh commands to different channels do not require stagger
3) tRFC_dlr must be met for refresh commands to different logical ranks within a package rank on the same channel
4) Any DRAM is considered to be in Refresh mode until tRFC time has been met
5) tCCD parameters must be met for Write and Write-Pattern commands to different logical ranks or physical ranks within the same channel; no overlapping write data bus activity is allowed on two physical or logical ranks within the same channel
6) Write and Write-Pattern commands to different channels do not require stagger
7) Each rank consists of one group of DRAMs making up a 36 or 40 bit channel (32 bits for non-ECC DIMMs)
8) These restrictions only apply to explicit all-banks refresh commands (REFab) and not to self-refresh entry or exit
9) Restrictions apply to DIMMs built with JEDEC PMICXXXX, but may not apply to DIMMs built with higher current capacity PMICs

19.0 PHYSICAL DIMENSIONS

19.1 2Gx8 based x80 Module (1 Rank) - M321R2GA3BB0

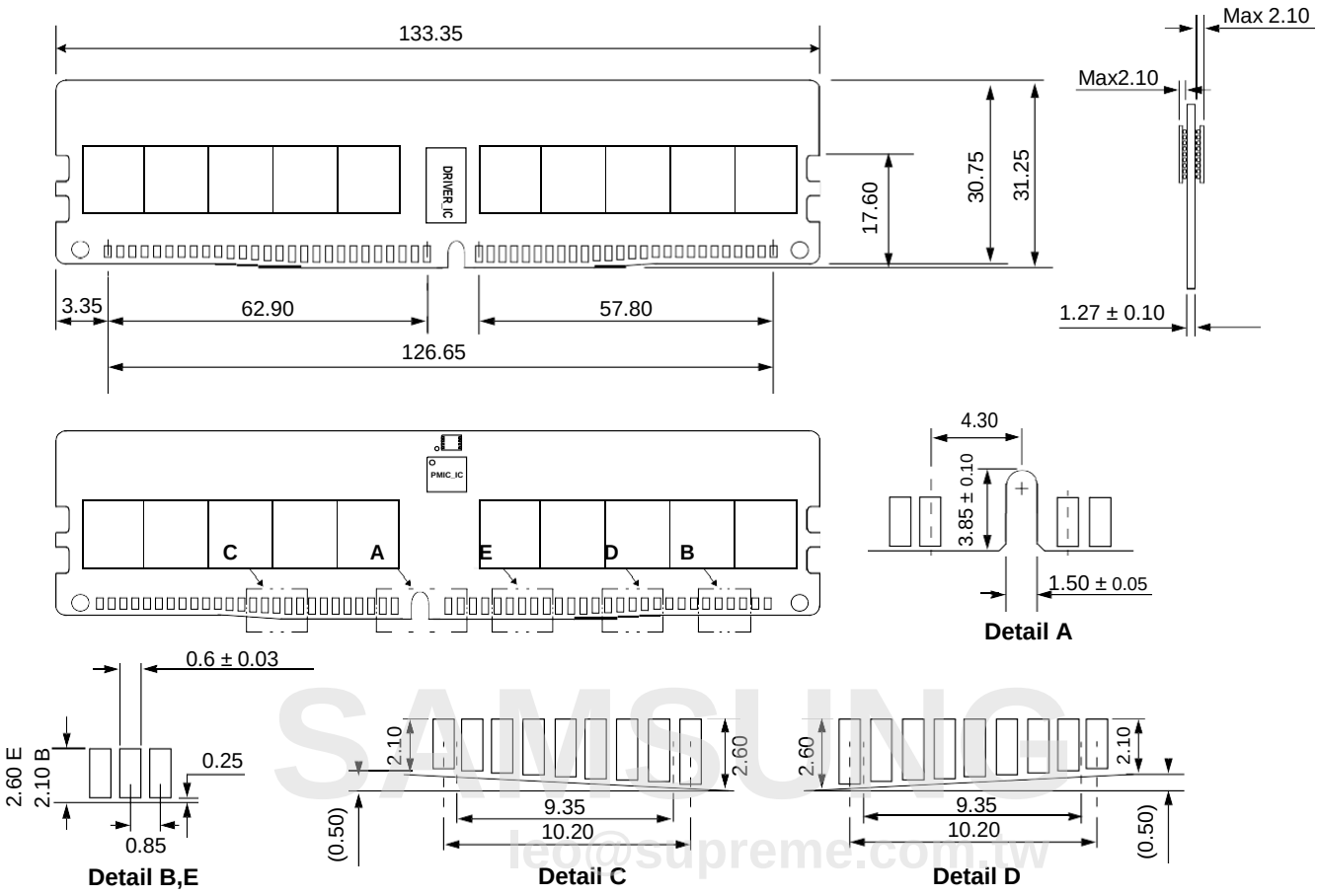
Units : mm



NOTE: Tolerances on all dimensions ±0.15 unless otherwise specified

19.2 2Gx8 based x80 Module (2 Ranks) - M321R4GA3BB0

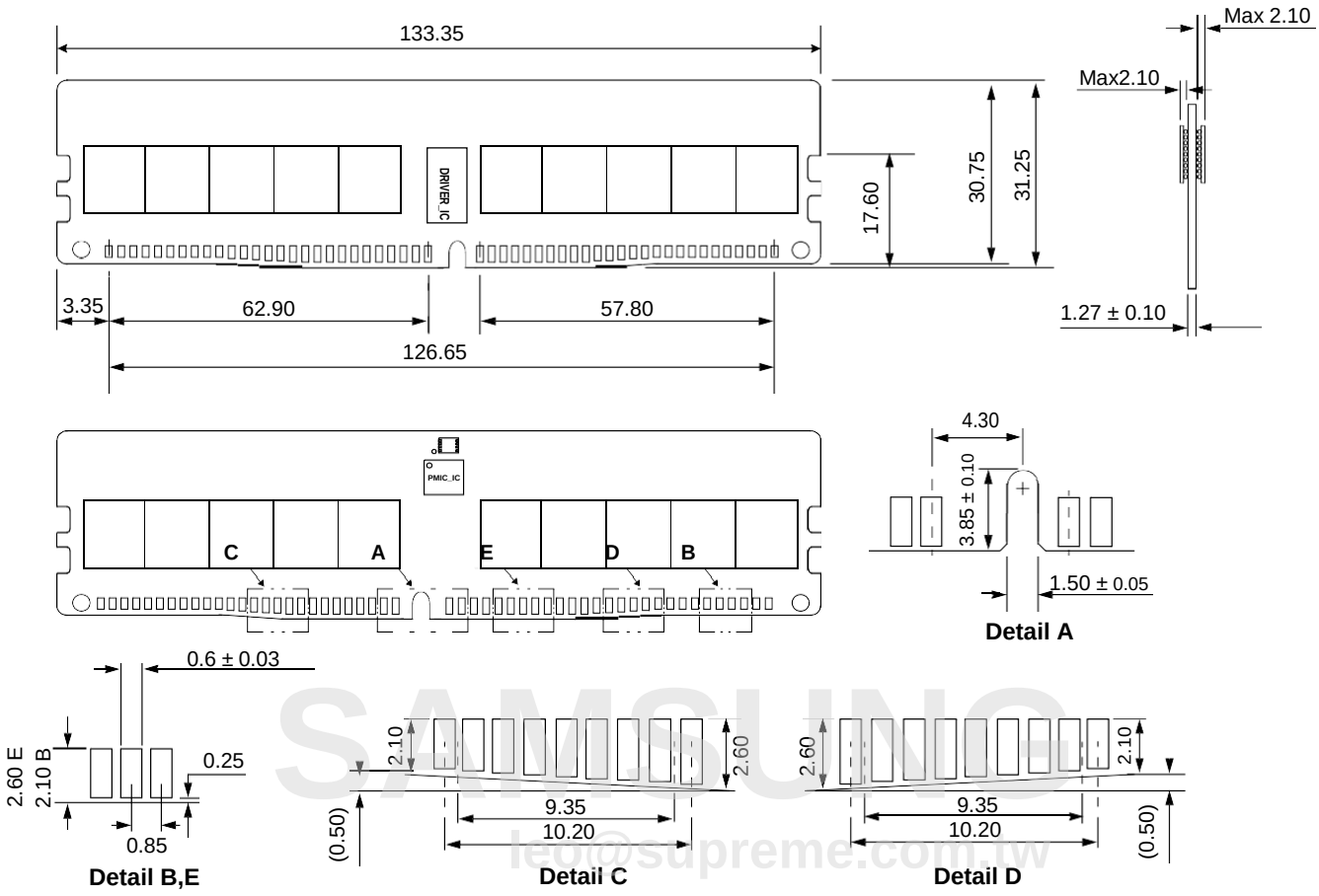
Units : mm



NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified

19.3 4Gx4 based x80 Module (1 Rank) - M321R4GA0BB0

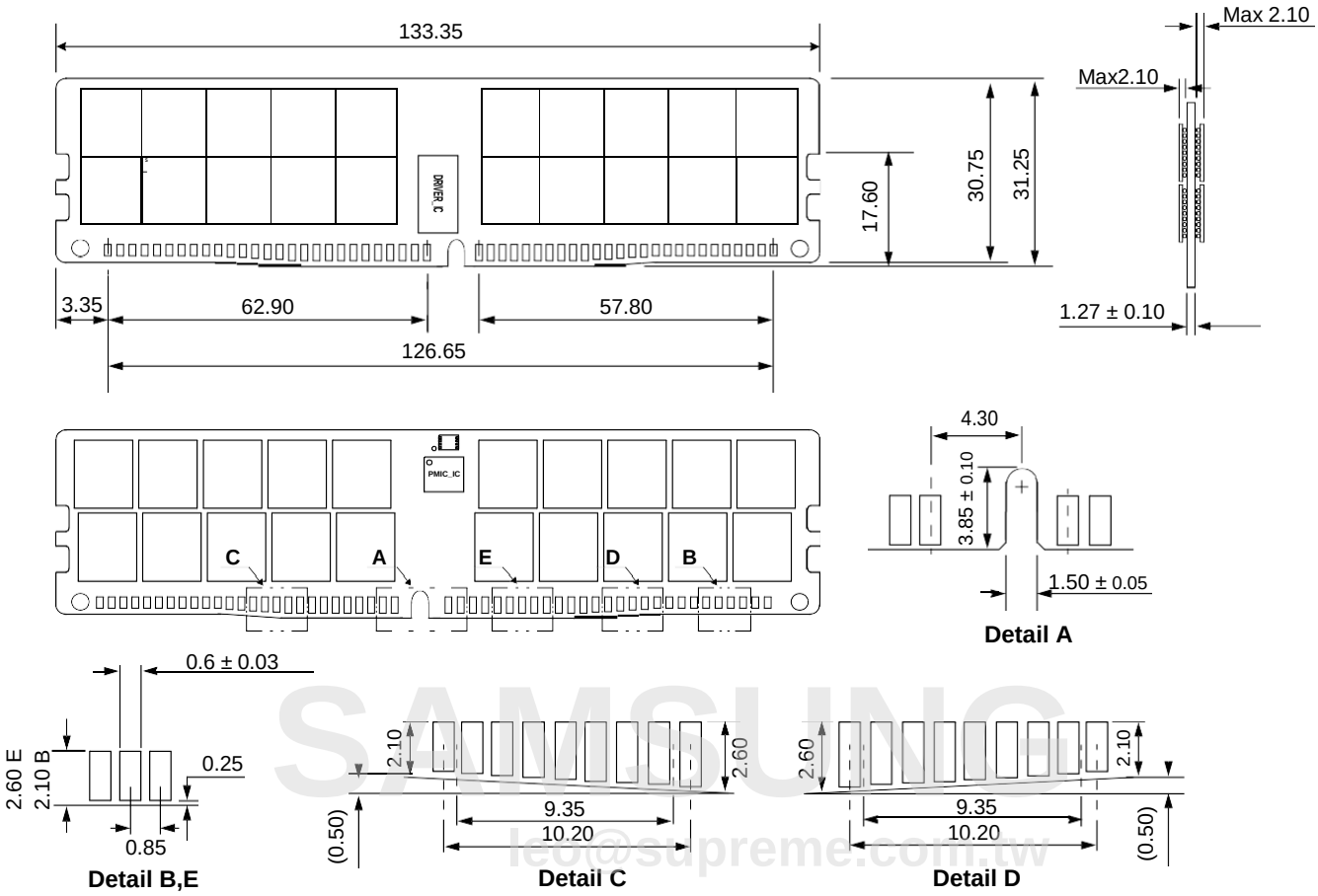
Units : mm



NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified

19.4 4Gx4 based x80 Module (2 Ranks) - M321R8GA0BB0

Units : mm



NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified

20.0 PRODUCT REGULATORY COMPLIANCE

20.1 Product Regulatory Compliance And Certifications

[Table 66] Samsung Module products comply with the following:

Category	Certifications	Region or Country	Standard
RoHS	CE	E.U. (Europe)	EN50581:2012

For more details are available at the following internet address:
https://www.samsung.com/semiconductor/about-us/global-compliance/

MANUFACTURER'S DECLARATION FOR CE CERTIFICATION

Hereby, Samsung Electronics declares that the product above is in compliance with Directive 2011/65/EU.

EU Compliance Contact information
Samsung Electronics (UK) Ltd, Euro QA Lab, Yateley, GU46 6GG. UK

Waste Electrical and Electronic Equipment

This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service, or the shop where you purchased the product.