

MZWLJ1T9HBJR-00007  
MZWLJ3T8HBLS-00007  
MZWLJ7T6HALA-00007  
MZWLJ15THALA-00007

# 2.5-inch PCIe SSD Specification (PM1733)

## datasheet

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## Revision History

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| 1.3                 | Modify Expansion Rom Register table(Table 40)                                                                                                                                                                                                                     | Apr. 08. 2020     | Revision      | Jay Kim       | Jay Kim         |

| Part Number        | Capacity <sup>1)</sup> | LBA (512 Bytes size) |
|--------------------|------------------------|----------------------|
| MZWLJ1T9HBJR-00007 | 1.92TB                 | 3,750,748,848        |
| MZWLJ3T8HBL5-00007 | 3.84TB                 | 7,501,476,528        |
| MZWLJ7T6HALA-00007 | 7.68TB                 | 15,002,931,888       |
| MZWLJ15THALA-00007 | 15.36TB                | 30,001,856,512       |

## NAND

- V5 256/512Gb NAND Flash Memory

## FEATURES

- PCI Express Gen3 / Gen4
- Single port x4 lanes/Dual port x2 lanes
- Enhanced Power-Loss Data Protection
- LDPC ECC
- End-to-End Data Protection
- Support Hot Plug/Removal
- Support up to 128 I/O Queues per Port
- Support Deallocate (a.k.a. TRIM) Command
- Support PCI Express AER (Advanced Error Reporting)
- Support 129 vectors for MSI-X
- Support SSD Enhanced S.M.A.R.T. Feature Set
- Hardware based AES-XTS 256-bit Encryption Engine
- Static and Dynamic Wear Leveling
- Support SFF-8639 SMBus
- Support NVMe-MI (Management Interface)
- Support Sanitize

## DRIVE CONFIGURATION

- Form Factor SFF-8639 2.5-inch
- Interface PCI Express Gen3/4 x4
- Bytes per Sector 512, 520, 4096, 4104, 4160 Bytes

## PERFORMANCE SPECIFICATIONS

### (1) Gen3

- Data Transfer Rate<sup>2</sup> (128KB data size)
  - Sequential Read/Write Up to 3,500/3,200 MB/s
- Data I/O Speed<sup>2</sup> (4KB data size, Sustained)
  - Random Read/Write Up to 800/135KIOPS
- Latency (Sustained random workload)
  - Read/Write (typical)<sup>3</sup> 100/25 us
  - Drive Ready Time (typical) Up to 4 sec
- Quality of service<sup>3</sup>
  - Read/Write (99%) 150/200 us

### (2) Gen4

- Data Transfer Rate<sup>2</sup> (128KB data size)
  - Sequential Read/Write Up to 7,000/3,800 MB/s
- Data I/O Speed<sup>2</sup> (4KB data size, Sustained)
  - Random Read/Write Up to 1500/135KIOPS
- Latency (Sustained random workload)
  - Read/Write (typical)<sup>3</sup> 100/25 us
  - Drive Ready Time (typical) Up to 4 sec
- Quality of service<sup>3</sup>
  - Read/Write (99%) 150/200 us

## COMPLIANCE

- PCI Express Base Specification Rev. 4.0
- NVMe Express Specification Rev. 1.3
- NVMe Express Management Interface Specification Rev. 1.0a

## CERTIFICATIONS AND DECLARATIONS

- cUL, CE, TUV-GS, CB, BSMI, KC, VCCI, Morocco, RCM, FCC, IC

## PRODUCT ECOLOGICAL COMPLIANCE

- RoHS

## RELIABILITY SPECIFICATIONS

- Uncorrectable Bit Error Rate 1 sector per 10<sup>17</sup> bits read
- MTBF 2,000,000 hours
- Power on Cycles (Ambient) 20,000
- Component Design Life 5 years
- Endurance 1 DWPD
- TBW (@8KB Random Write)
  - 1.92TB 3.504 PB
  - 3.84TB 7.008 PB
  - 7.68TB 14.016 PB
  - 15.36TB 28.032 PB
- Data Retention 3 months

## ENVIRONMENTAL SPECIFICATIONS

- Temperature, Case (TC<sup>4</sup>)
  - Operating 0 ~ 70 °C
  - Non-operating<sup>5</sup> -40 ~ 85 °C
- Humidity (Non-operating) 5 ~ 95%
- Shock 1,500 G / 0.5msec
- Vibration
  - Sinusoidal 20 Gpeak, 10 ~ 2000Hz

## POWER REQUIREMENTS

- Supply Voltage / Tolerance 12V±10%
- Active<sup>6</sup> (max. RMS) Up to 22 W
- Idle<sup>6</sup> (typ.) 8.5 W

## PHYSICAL DIMENSION

- Width 69.85 ± 0.25 mm
- Length 100.20 ± 0.25 mm
- Height 15.00 + 0.00 / - 0.50 mm
- Weight Up to 190 g

## OPERATING SYSTEMS

Windows Server 2012 R2 64-bit  
Windows Server 2016  
Windows Server 2019  
RHEL 7.5 (Kernel 3.10.0)  
CentOS 7.5 (Kernel 3.10.0)  
SLES 12 (Kernel 3.12.61)

NOTE: Specifications are subject to change without notice.

- 1) 1MB = 1,000,000 Bytes, 1GB = 1,000,000,000 Bytes, unformatted Capacity. User accessible capacity may vary depending on operating environment and formatting.
- 2) Based on PCI Express Gen3 x4, Random performance measured using FIO in Ubuntu 17.10 with queue depth 64 by 4 workers(Jobs) and Sequential performance with queue depth 64 by 1 worker.Also, Based on PCI Express Gen4 x4 Random performance measured using FIO in Ubuntu 17.10 with queue depth 64 by 16 workers(Jobs) and Sequential performance with queue depth 64 by 1 worker.Actual performance may vary depending on use conditions and environment.
- 3) The read/write latency and Quality of Service are measured by using FIO in Ubuntu 17.10 and 4KB transfer size with queue depth 1 on a random workload of sustained state.
- 4) Tc is measured at the hottest point on the case with sufficient airflow condition such as 2.5CFM or more at 25°C of ambient temperature.
- 5) Storing (or shipping) without power connection.
- 6) The values (Active/Idle power) are based on estimates.

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## 1.0 INTRODUCTION

### 1.1 General Description

This document describes the specifications of the Samsung SSD PM1733, which is a native-PCIe SSD for enterprise application. The Samsung SSD PM1733 presents outstanding performance with instant responsiveness to the host system, by applying the Peripheral Component Interconnect Express (PCIe) 4.0 interface standard, as well as highly efficient Non-Volatile Memory Express (NVMe) Protocol. The Samsung SSD PM1733 delivers wide bandwidth of 7.0GB/s for sequential read speed and 3.8GB/s for sequential write speed under 22W power. With the help of Toggle 4.0 NAND Flash interface, the Samsung SSD PM1733 delivers latency of 100us for random 4KB read of 1500KIOPs and 25us for random 4KB write of 135KIOPs in the sustained state. By combining the enhanced reliability Samsung NAND Flash memory silicon with NAND Flash management technologies, the Samsung SSD PM1733 delivers the extended endurance of up to 1 Drive Writes Per Day (DWPD) for 5 years, which is suitable for enterprise applications, in one 2.5-inch form factor lineup: 1.92TB, 3.84TB, 7.68TB, 15.36TB. In addition, the Samsung SSD PM1733 supports Hot Plug insertion and removal feature by employing the efficient circuitry for Power Loss Protection (PLP) and handling inrush current. PLP solution can guarantee that data issued by the host system are written to the storage media without any loss in the event of sudden power off or sudden power failure. Inrush current handler can protect the internal components from the electrical and physical damages.

### 1.2 Product List

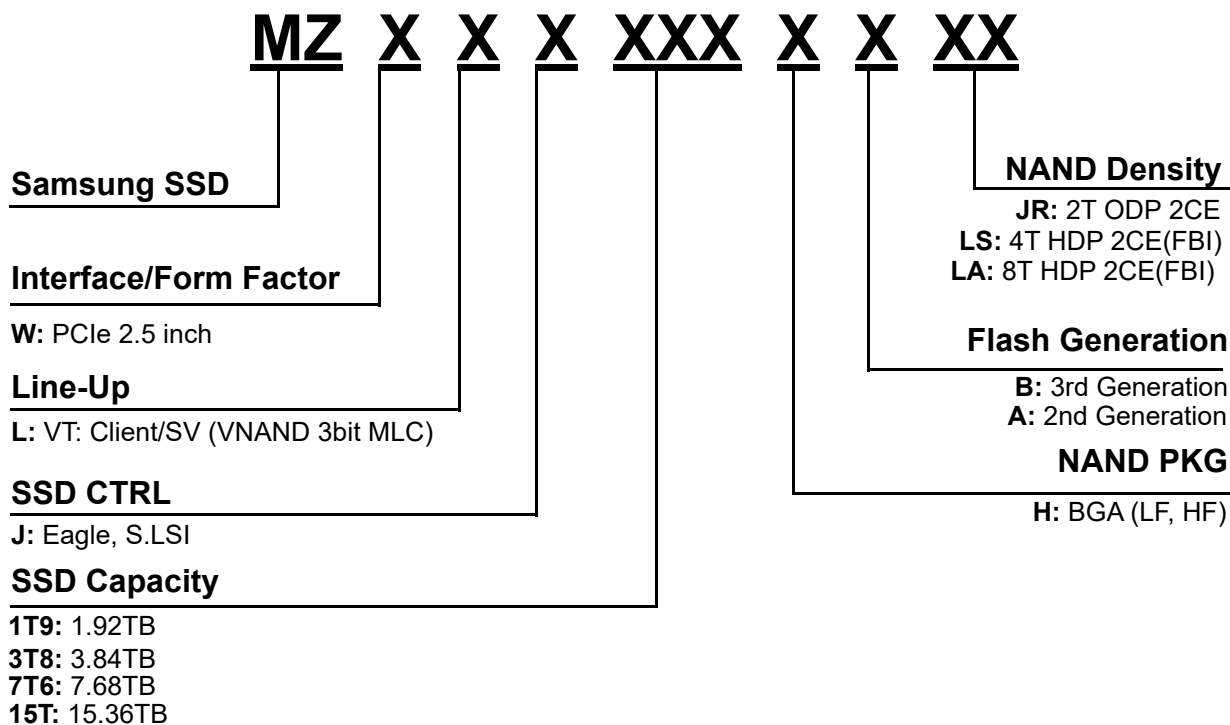
[Table 1] Product List

| Type                   | Capacity | Part Number        |
|------------------------|----------|--------------------|
| 2.5-inch <sup>1)</sup> | 1.92TB   | MZWLJ1T9HBJR-00007 |
|                        | 3.84TB   | MZWLJ3T8HBLS-00007 |
|                        | 7.68TB   | MZWLJ7T6HALA-00007 |
|                        | 15.36TB  | MZWLJ15THALA-00007 |

**NOTE:**

1) SFF-8639 combo (SATA, SAS, PCIe) standard connector

### 1.3 Ordering Information



## 2.0 PRODUCT SPECIFICATIONS

### 2.1 Capacity

[Table 2] User Capacity and Addressable Sectors

| Capacity <sup>2)</sup> | Max LBA <sup>3)</sup> |
|------------------------|-----------------------|
| 1.92TB                 | 3,750,748,848         |
| 3.84TB                 | 7,501,476,528         |
| 7.68TB                 | 15,002,931,888        |
| 15.36TB                | 30,001,856,512        |

**NOTE:**

1) Gigabyte (GB) = 1,000,000,000 Bytes, 1 Sector = 4160Bytes

2) Capacity shown in Table 2 represents the total usable capacity of the SSD which may be less than the total physical capacity. A certain area in physical capacity, not in the area shown to the user, might be used for the purpose of NAND flash management.

3) Max. LBA shown in Table 2 represents the total user addressable sectors in LBA mode and calculated by IDEMA.

### 2.2 Performance

[Table 3] Sustained Random Read/Write Performance (IOPS)

| Maximum Performance <sup>1)</sup> |                  | Unit | 1.92TB | 3.84TB | 7.68TB | 15.36TB |
|-----------------------------------|------------------|------|--------|--------|--------|---------|
| PCIe Gen3                         | Random 4KB Read  | IOPS | 800K   | 800K   | 800K   | 800K    |
|                                   | Random 4KB Write | IOPS | 100K   | 135K   | 135K   | 135K    |
| PCIe Gen4                         | Random 4KB Read  | IOPS | 800K   | 1500K  | 1450K  | 1450K   |
|                                   | Random 4KB Write | IOPS | 100K   | 135K   | 135K   | 135K    |

**NOTE:**

1) Random performance in Table 3 PCIe GEN3 was measured as dual port by using FIO in Ubuntu 17.10 with queue depth 64 by 4 workers(Jobs) to each port. Measurements were performed on half capacity offset to 2nd port. Random performance in Table 3 PCIe GEN4 was measured as single Port by using FIO in Ubuntu 17.10 with queue depth 64 by 16 workers(Jobs) Actual performance may vary depending on use conditions and environment.

[Table 4] Sequential Read/Write Performance

| Maximum Performance <sup>1)</sup> |                        | Unit | 1.92TB | 3.84TB | 7.68TB | 15.36TB |
|-----------------------------------|------------------------|------|--------|--------|--------|---------|
| PCIe Gen3                         | Sequential 128KB Read  | MB/s | 3,500  | 3,500  | 3,500  | 3,500   |
|                                   | Sequential 128KB Write | MB/s | 2,400  | 3,200  | 3,200  | 3,200   |
| PCIe Gen4                         | Sequential 128KB Read  | MB/s | 7,000  | 7,000  | 7,000  | 7,000   |
|                                   | Sequential 128KB Write | MB/s | 2,400  | 3,800  | 3,800  | 3,800   |

**NOTE:**

1) Sequential performance in Table 4 PCIe GEN3 was measured as dual port by using FIO in Ubuntu 17.10 with queue depth 64 by 1 worker(Job) to each port. Measurements were performed on half capacity offset to 2nd port. Sequential performance in Table 4 PCIe GEN4 was measured as single port by using FIO in Ubuntu 17.10 with queue depth 64 by 1 worker(Job). Actual performance may vary depending on use conditions and environment.

### 2.3 Latency

[Table 5] Latency<sup>1)</sup> (sustained state)

| Queue Depth = 1                |                                     | Unit | 1.92TB  | 3.84TB  | 7.68TB  | 15.36TB |
|--------------------------------|-------------------------------------|------|---------|---------|---------|---------|
| PCIe Gen3                      | 4KB Random Read/Write <sup>2)</sup> | us   | 100/25  | 100/25  | 100/25  | 100/25  |
|                                | Sequential Read/Write <sup>3)</sup> | us   | 250/100 | 250/100 | 250/100 | 250/100 |
| PCIe Gen4                      | 4KB Random Read/Write <sup>2)</sup> | us   | 100/25  | 100/25  | 100/25  | 100/25  |
|                                | Sequential Read/Write <sup>3)</sup> | us   | 220/80  | 220/80  | 220/80  | 220/80  |
| Drive Ready Time <sup>4)</sup> |                                     | sec  | 2       | 2       | 3       | 4       |

**NOTE:**

1) Typical values.

2) The random read/write latency is measured by using FIO in Ubuntu 17.10 and 4KB transfer size with queue depth 1 on a random workload of sustained state.

3) The sequential read/write latency is measured by using FIO in Ubuntu 17.10 and 128KB transfer size with queue depth 1 on a sequential workload of sustained state.

4) The maximum taking time to be ready for receiving commands after power-up (CSTS.Ready=1). It is expected that I/O commands may not be completed at this point.

## 2.4 Quality of Service (QoS)

[Table 6] Quality of Service (QoS)

| Quality of Service (99%) |                         | Unit | 1.92TB | 3.84TB | 7.68TB | 15.36TB |
|--------------------------|-------------------------|------|--------|--------|--------|---------|
| PCIe Gen3                | Read(4KB)(QD=1,Job=1)   | us   | 150    | 150    | 150    | 150     |
|                          | Write(4KB)(QD=1,Job=1)  | us   | 200    | 200    | 200    | 200     |
|                          | Read(4KB)(QD=64,Job=4)  | ms   | 3      | 3      | 3      | 3       |
|                          | Write(4KB)(QD=64,Job=4) | ms   | 10     | 10     | 10     | 10      |
| PCIe Gen4                | Read(4KB)(QD=1,Job=1)   | us   | 150    | 150    | 150    | 150     |
|                          | Write(4KB)(QD=1,Job=1)  | us   | 200    | 200    | 200    | 200     |
|                          | Read(4KB)(QD=64,Job=4)  | ms   | 3      | 3      | 3      | 3       |
|                          | Write(4KB)(QD=64,Job=4) | ms   | 10     | 10     | 10     | 10      |

| Quality of Service (99.99%) |                         | Unit | 1.92TB | 3.84TB | 7.68TB | 15.36TB |
|-----------------------------|-------------------------|------|--------|--------|--------|---------|
| PCIe Gen3                   | Read(4KB)(QD=1,Job=1)   | us   | 220    | 220    | 220    | 220     |
|                             | Write(4KB)(QD=1,Job=1)  | us   | 450    | 450    | 450    | 450     |
|                             | Read(4KB)(QD=64,Job=4)  | ms   | 5      | 5      | 5      | 5       |
|                             | Write(4KB)(QD=64,Job=4) | ms   | 20     | 20     | 20     | 20      |
| PCIe Gen4                   | Read(4KB)(QD=1,Job=1)   | us   | 220    | 220    | 220    | 220     |
|                             | Write(4KB)(QD=1,Job=1)  | us   | 450    | 450    | 450    | 450     |
|                             | Read(4KB)(QD=64,Job=4)  | ms   | 5      | 5      | 5      | 5       |
|                             | Write(4KB)(QD=64,Job=4) | ms   | 20     | 20     | 20     | 20      |

**NOTE:**  
1) QoS is measured using FIO (99/99.99 %) with queue depth 1, Job=1 on single port and queue depth 64, Job=4 for single port on 4KB random and write.  
2) QoS is measured as the maximum round-trip time taken for 99 % of commands to host.  
3) QoS is measured as the maximum round-trip time taken for 99.99 % of commands to host.

## 2.5 IOPS Consistency

[Table 7] IOPS Consistency

| IOPS Consistency <sup>1, 2</sup> | Unit | 1.92TB | 3.84TB | 7.68TB | 15.36TB |
|----------------------------------|------|--------|--------|--------|---------|
| Random Read (4 KB)               | %    | 95     | 95     | 95     | 95      |
| Random Write (4 KB)              | %    | 90     | 90     | 90     | 90      |
| Random Read (8 KB)               | %    | 95     | 95     | 95     | 95      |
| Random Write (8 KB)              | %    | 90     | 90     | 90     | 90      |

**NOTE:**  
1) IOPS consistency measured using FIO with queue depth 128, worker 4 on 1 port over dual port condition.  
2) IOPS Consistency (%) = (IOPS in the 99.9% slowest 1-second interval)/(average IOPS during the test).

## 2.6 Power

The Samsung SSD PM1733 is implemented in standardized 2.5-inch form factor and gets primary 12V power as well as auxiliary 3.3V (3.3Vaux) power through the indicated pins (#P13~15 for 12V and #E3 for 3.3Vaux in SFF-8639 connector plug) from the host system.  
For 12V and 3.3Vaux, the allowable voltage tolerance and noise level in SSD are described in chapter 2.5.1, the power consumption in 2.5.2 and the inrush current in 2.7.2.

### 2.6.1 Maximum Voltage Ratings (12V and 3.3Vaux)

[Table 8] Allowable Voltage Tolerance<sup>1</sup>

| Operating Voltage                    | 1.92TB                                                 | 3.84TB | 7.68TB | 15.36TB |
|--------------------------------------|--------------------------------------------------------|--------|--------|---------|
| 12V <sup>2</sup>                     | 10%                                                    |        |        |         |
| 12V Rise time (Max/Min)              | 100ms/1ms                                              |        |        |         |
| 12V Fall time (Max/Min) <sup>4</sup> | 5s/1ms                                                 |        |        |         |
| 12V Noise level                      | 1000 mV pp 10Hz – 100 KHz<br>100 mV pp 100KHz – 20 MHz |        |        |         |

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|                                          |                                                      |
|------------------------------------------|------------------------------------------------------|
| 3.3Vaux <sup>3</sup>                     | 10%                                                  |
| 3.3Vaux Rise time (Max/Min)              | 50ms/1ms                                             |
| 3.3Vaux Fall time (Max/Min) <sup>4</sup> | 5s/1ms                                               |
| 3.3Vaux Noise level                      | 300 mV pp 10Hz – 100 KHz<br>50 mV pp 100KHz – 20 MHz |

**NOTE:**  
1) The components inside SSD were designed to endure the range of voltage fluctuations, which might be induced by the host system, in Table 8.  
2) For 12V operating voltage, the minimum allowable is 10.8V and the maximum 13.2V.  
3) For 3.3Vaux, the minimum allowable voltage is 2.97V and the maximum 3.63V.  
4) Fall time needs to be equal or better than minimum in order to guarantee full functionality of enhanced power loss management.

## 2.6.2 Power Consumption (12V)

In enterprise server and storage system, the Samsung SSD PM1733 is designed for the specific usage, which means that SSD will be always operated by the host system during the entire life. Hence, the Samsung SSD PM1733 does not manage any low power modes except for the Active/Idle, Off mode.

[Table 9] Power Consumption (12V Supply Voltage)<sup>1</sup>

| Power Mode |                     |       | 1.92TB | 3.84TB | 7.68TB | 15.36TB |
|------------|---------------------|-------|--------|--------|--------|---------|
| PCIe Gen3  | Active <sup>2</sup> | Read  | 15W    | 15W    | 15W    | 15W     |
|            |                     | Write | 15W    | 20W    | 20W    | 20W     |
|            | Idle <sup>3</sup>   |       | 8.5W   | 8.5W   | 8.5W   | 8.5W    |
|            | Off                 |       | 0W     | 0W     | 0W     | 0W      |
| PCIe Gen4  | Active <sup>2</sup> | Read  | 15W    | 20W    | 20W    | 20W     |
|            |                     | Write | 15W    | 20W    | 20W    | 22W     |
|            | Idle <sup>3</sup>   |       | 8.5W   | 8.5W   | 8.5W   | 8.5W    |
|            | Off                 |       | 0W     | 0W     | 0W     | 0W      |

**NOTE:**  
1) Power consumption was measured in the 12V power pins (#P13~#P15) of the connector plug in SSD. The active and idle power is defined as the highest averaged power value, which is the maximum RMS average value over 100 ms duration.  
2) The measurement condition for active power is assumed for maximum power between sequential or random performance.  
3) The idle state is defined as the state that the host system can issue any commands into SSD at any time.

## 2.7 Reliability

The reliability specification of the Samsung SSD PM1733 follows JEDEC standard, which are included in JESD218A and JESD219A documents.

### 2.7.1 Mean Time Between Failures

By definition, Mean Time between Failures (MTBF) is the estimated time between failures occurring during SSD operation.

[Table 10] MTBF Specifications

| Parameter | 1.92TB          | 3.84TB | 7.68TB | 15.36TB |
|-----------|-----------------|--------|--------|---------|
| MTBF      | 2,000,000 Hours |        |        |         |

### 2.7.2 Uncorrectable Bit Error Rate

By definition, Uncorrectable Bit Error Rate (UBER) is a metric for the rate of occurrence of data errors, equal to the number of data errors per bits read as specified in the JESD218 document of JEDEC standard.

[Table 11] UBER Specifications

| Parameter | 1.92TB                                  | 3.84TB | 7.68TB | 15.36TB |
|-----------|-----------------------------------------|--------|--------|---------|
| UBER      | 1 sector per 10 <sup>17</sup> bits read |        |        |         |

**NOTE:**  
1) For the enterprise application, JEDEC recommends that UBER shall be below 10<sup>-16</sup>

### 2.7.3 Data Retention

By definition, data retention is the expected time period for retaining data in the SSD at the maximum rated endurance in power-off state as specified in the JESD218 document of JEDEC standard.

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[Table 12] Data Retention

| Parameter                   | 1.92TB   | 3.84TB | 7.68TB | 15.36TB |
|-----------------------------|----------|--------|--------|---------|
| Data Retention <sup>1</sup> | 3 months |        |        |         |

**NOTE:**

1) Data retention was measured by assuming that SSD reaches the maximum rated endurance at 40°C in power-off state.

## 2.7.4 Endurance

By definition, the endurance of SSD in enterprise application is defined as the maximum number of drive writes per day that can meet the requirements specified in the JESD218 document of JEDEC standard.

[Table 13] Drive Write Per Day (DWPD)

| Parameter | 1.92TB                              | 3.84TB | 7.68TB | 15.36TB |
|-----------|-------------------------------------|--------|--------|---------|
| DWPD      | 1 drive writes per day over 5 years |        |        |         |

[Table 14] Petabyte Written (PBW)

| Parameter | Unit | 1.92TB | 3.84TB | 7.68TB | 15.36TB |
|-----------|------|--------|--------|--------|---------|
| PBW       | PB   | 3.504  | 7.008  | 14.016 | 28.032  |

**NOTE:**

1) Relational formula between DWPD and PBW is like below:

PBW = DWPD x 365 x 5 x User capacity

2) PBW was calculated at 4KB random write.

## 2.8 Hot Plug Support

### 2.8.1 Power Loss Protection

By using internal back-up power technology, the Samsung SSD PM1733 supports power loss protection (PLP) feature to guarantee the reliability of data requested by the host system. When power is unpredictably lost, SSD can detect automatically this abnormal situation and transfer all user data and meta-data cached in DRAM into the Flash media during any SSD operations.

### 2.8.2 Inrush Current Protection

When the Samsung SSD PM1733 plugs in the backplane of host system, the significant amount of current is induced through 12V power rail. The Samsung SSD PM1733 has protection circuitry including a set of resistors and capacitors to alleviate the impact by inrush current through 12V power.

[Table 15] Inrush Current

| Inrush Current | 1.92TB             | 3.84TB | 7.68TB | 15.36TB |
|----------------|--------------------|--------|--------|---------|
| 12 V           | 1.8A <sup>1)</sup> |        |        |         |

**NOTE:**

1) The measurement value of inrush current is also compatible with the standard specification of "Enterprise SSD Form Factor Version 1.0a" released by SSD Form Factor Working Group.

## 2.9 Environmental Specification

### 2.9.1 Temperature

[Table 16] Temperature, Case (Tc<sup>1</sup>)

|                           |                             | 1.92TB       | 3.84TB | 7.68TB | 15.36TB |
|---------------------------|-----------------------------|--------------|--------|--------|---------|
| Temperature <sup>1)</sup> | Operating                   | 0 to 70 °C   |        |        |         |
|                           | Non-Operating <sup>2)</sup> | -40 to 85 °C |        |        |         |

**NOTE:**

1) Tc is measured at the hottest point on the case with sufficient airflow condition such as 2.5CFM or more at 25 °C of ambient temperature.

2) Storing (or shipping) without power connection.

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## 2.9.2 Humidity

[Table 17] Humidity

|                       |               | 1.92TB    | 3.84TB | 7.68TB | 15.36TB |
|-----------------------|---------------|-----------|--------|--------|---------|
| Humidity <sup>1</sup> | Non-operating | 5% to 95% |        |        |         |

**NOTE:**

1) Humidity is measured in non-condensing state.

## 2.9.3 Shock and Vibration

[Table 18] Shock and Vibration

|                        |               | 1.92TB                            | 3.84TB | 7.68TB | 15.36TB |
|------------------------|---------------|-----------------------------------|--------|--------|---------|
| Shock <sup>1</sup>     | Non-operating | 1,500G                            |        |        |         |
| Vibration <sup>2</sup> | Non-operating | 20 Gpeak (10~2,000Hz, Sweep sine) |        |        |         |

**NOTE:**

1) Shock specifications assume that SSD shall be mounted with screws when input vibration is applied. Vibration may be applied in 3 axes (x, y and z) with a half sine waveform of 0.5ms duration in non-operating condition.

2) Vibration specifications assume that SSD shall be mounted with screws when input vibration is applied. The input vibration may be applied in 3 axes (x, y and z) and lasts during 15 minutes per axis.

## 3.0 MECHANICAL SPECIFICATIONS

### 3.1 Physical Information

The physical case of the Samsung SSD PM1733 in 2.5-inch form factor follows the standardized dimensions defined by SSD Form Factor Work Group.

[Table 19] Physical Dimensions and Weight

| Parameter | Unit | 1.92TB             | 3.84TB | 7.68TB | 15.36TB |
|-----------|------|--------------------|--------|--------|---------|
| Width     | mm   | 69.85±0.25         |        |        |         |
| Length    | mm   | 100.20±0.25        |        |        |         |
| Thickness | mm   | 15.00 + 0.00/-0.50 |        |        |         |
| Weight    | g    | Up to 190g         |        |        |         |

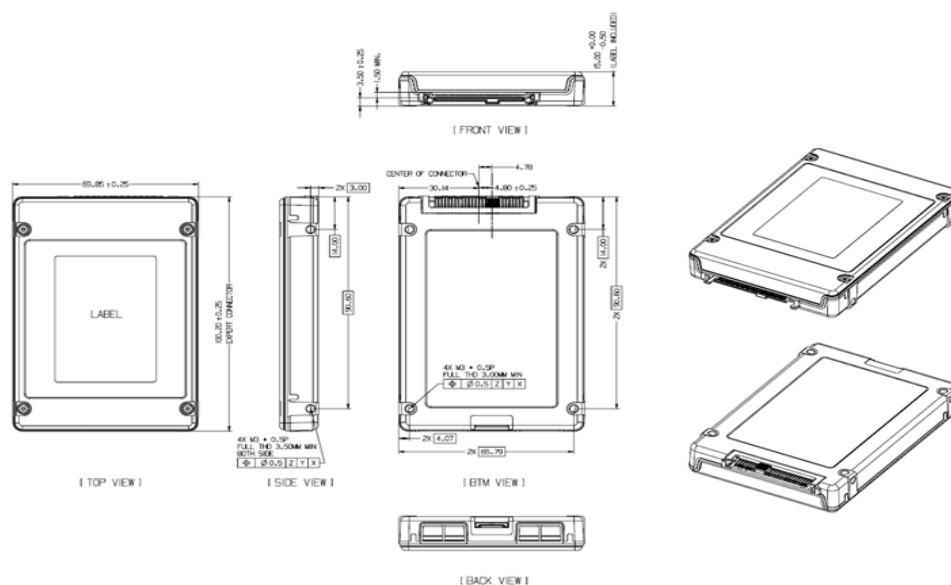


Figure 1. Mechanical Outline (1PCB Product)  
(MZWLJ1T9HBJR-00007, MZWLJ3T8HBLS-00007, MZWLJ7T6HALA-00007)

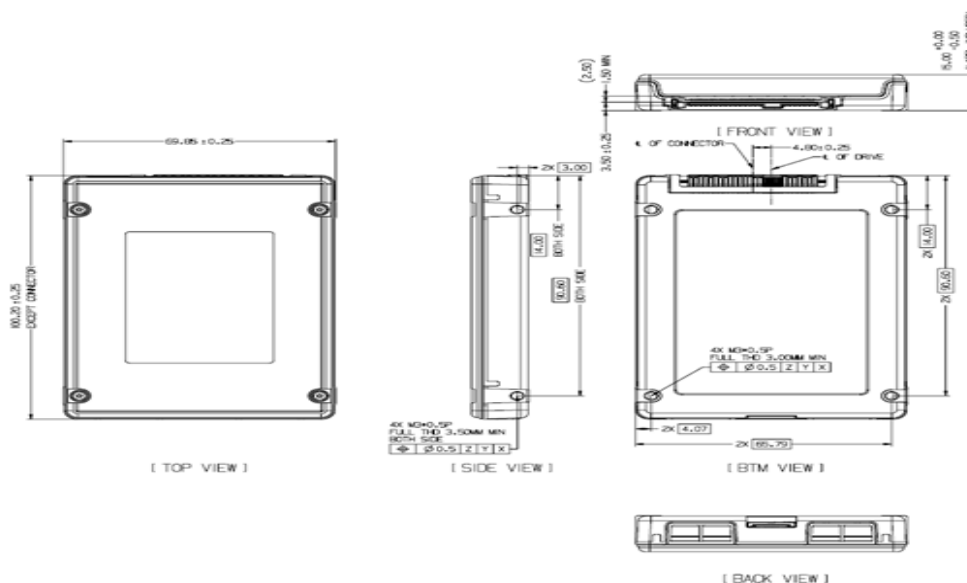


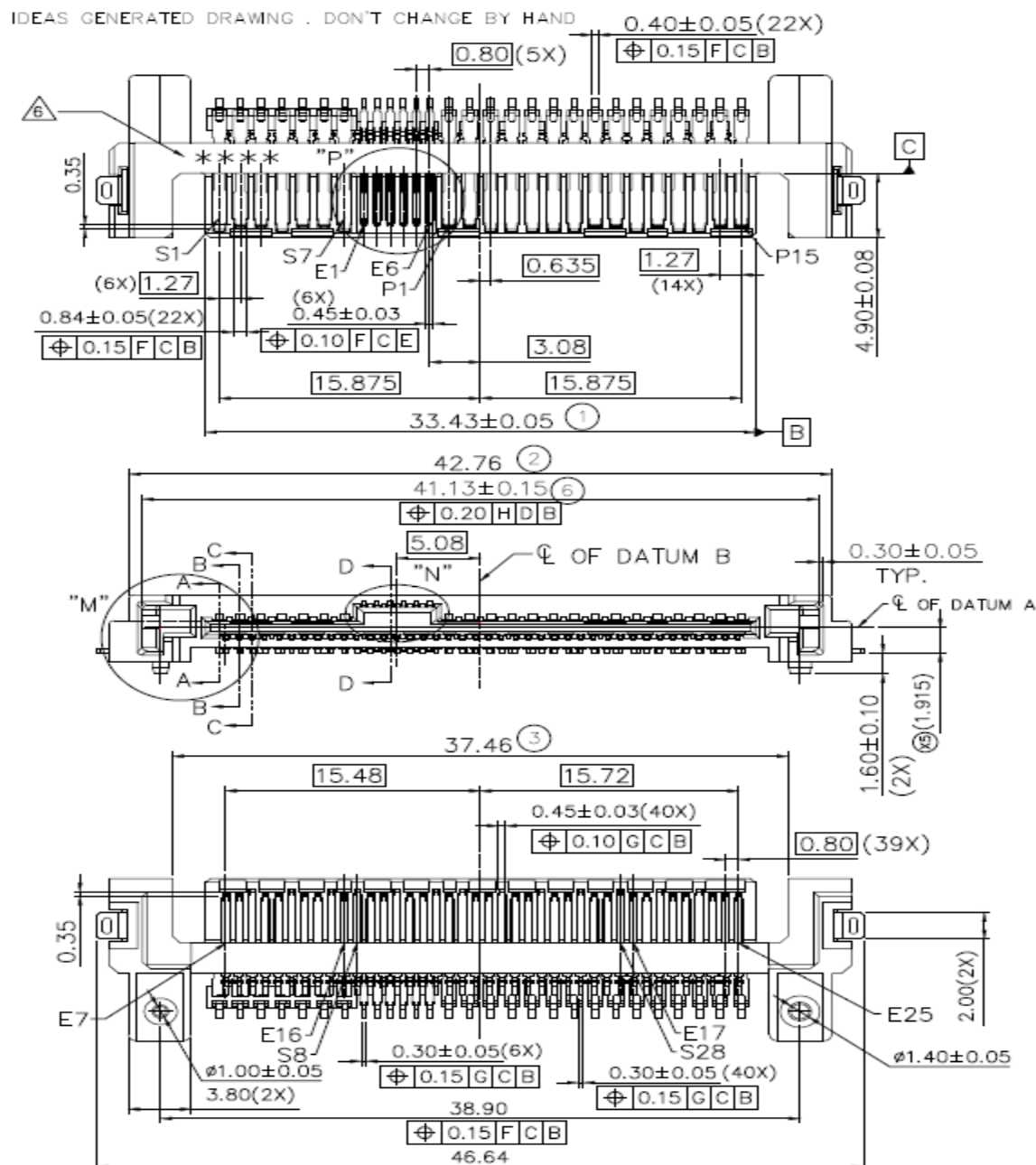
Figure 2. Mechanical Outline (2PCB Product)  
(MZWLJ15THALA-00007)

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## 4.0 INTERFACE SPECIFICATION

The PCIe connector of PM1733 is compliant with SFF-8639 standard specification.

### 4.1 Connector Dimensions



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## 4.2 Connector Pin Assignments

[Table 20] Certifications and Declarations

| Pin# | Assignment    | Description                                | Pin# | Assignment | Description                             |
|------|---------------|--------------------------------------------|------|------------|-----------------------------------------|
| S1   | Gnd           | GND                                        | E7   | REFCLK+    | PCIe Reference Clock + (primary port A) |
| S2   | Not Used      | Float                                      | E8   | REFCLK-    | PCIe Reference Clock - (primary port A) |
| S3   | Not Used      | Float                                      | E9   | Gnd        | GND                                     |
| S4   | GND           | GND                                        | E10  | PETp0      | PCIe Transmit+ (lane 0)                 |
| S5   | Not Used      | Float                                      | E11  | PETn0      | PCIe Transmit- (lane 0)                 |
| S6   | Not Used      | Float                                      | E12  | Gnd        | GND                                     |
| S7   | Gnd           | GND                                        | E13  | PERn0      | PCIe Receive- (lane 0)                  |
| E1   | RFECLK+       | PCIe Reference Clock + (dual port, port B) | E14  | PERp0      | PCIe Receive+ (lane 0)                  |
| E2   | RFECLK-       | PCIe Reference Clock - (dual port, port B) | E15  | Gnd        | GND                                     |
| E3   | 3.3Vaux       | Auxiliary Power (for SMBus access)         | E16  | Not Used   | Float                                   |
| E4   | PERSTB#       | PCIe Reset (dual port, port B)             | S8   | Gnd        | GND                                     |
| E5   | PERST#        | PCIe Reset (primary port A)                | S9   | Not Used   | Float                                   |
| E6   | Not Used      | Float                                      | S10  | Not Used   | Float                                   |
| P1   | Not Used      | Float                                      | S11  | Gnd        | GND                                     |
| P2   | Not Used      | Float                                      | S12  | Not Used   | Float                                   |
| P3   | PWRDIS        | Power Disable                              | S13  | Not Used   | Float                                   |
| P4   | IFDET#        | Interface Detect                           | S14  | Gnd        | GND                                     |
| P5   | Gnd           | GND                                        | S15  | Not Used   | Float                                   |
| P6   | Gnd           | GND                                        | S16  | Gnd        | GND                                     |
| P7   | Not Used      | Float                                      | S17  | PETp1      | PCIe Transmit+ (lane 1)                 |
| P8   | Not Used      | Float                                      | S18  | PETn1      | PCIe Transmit- (lane 1)                 |
| P9   | Not Used      | Float                                      | S19  | Gnd        | GND                                     |
| P10  | Not Used      | Presence                                   | S20  | PERn1      | PCIe Receive- (lane 1)                  |
| P11  | Activity      | Drive Active                               | S21  | PERp1      | PCIe Receive+ (lane 1)                  |
| P12  | Gnd           | GND                                        | S22  | Gnd        | GND                                     |
| P13  | Precharge 12V | Primary Power                              | S23  | PETp2      | PCIe Transmit+ (lane 2)                 |
| P14  | 12V           | Primary Power                              | S24  | PETn2      | PCIe Transmit- (lane 2)                 |
| P15  | 12V           | Primary Power                              | S25  | Gnd        | GND                                     |
|      |               |                                            | S26  | PERn2      | PCIe Receive- (lane 2)                  |
|      |               |                                            | S27  | PERp2      | PCIe Receive+ (lane 2)                  |
|      |               |                                            | S28  | Gnd        | GND                                     |
|      |               |                                            | E17  | PETp3      | PCIe Transmit+ (lane 3)                 |
|      |               |                                            | E18  | PETn3      | PCIe Transmit- (lane 3)                 |
|      |               |                                            | E19  | Gnd        | GND                                     |
|      |               |                                            | E20  | PERn3      | PCIe Receive- (lane 3)                  |
|      |               |                                            | E21  | PERp3      | PCIe Receive+ (lane 3)                  |
|      |               |                                            | E22  | Gnd        | GND                                     |

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|  |  |  |     |              |                       |
|--|--|--|-----|--------------|-----------------------|
|  |  |  | E23 | SMCLK        | SMBus Clock           |
|  |  |  | E24 | SMDAT        | SMBus Data            |
|  |  |  | E25 | DualLink En# | Dual Port PCIe enable |

## 5.0 PCI AND NVM EXPRESS REGISTERS

### 5.1 PCI Express Configuration Registers

#### 5.1.1 PCI Register Summary

[Table 21] PCI Register Summary

| Start Address | Tag        | Name                                               | Type                           |
|---------------|------------|----------------------------------------------------|--------------------------------|
| 00h           | TYPE0_HDR  | PCI Header                                         | PCI Configuration Header Space |
| 40h           | PM_CAP     | PCI Power Management Capability                    | PCI Capability                 |
| 70h           | PCIE_CAP   | PCI Express Capability                             | PCI Capability                 |
| B0h           | MSIX_CAP   | MSI-X Capability                                   | PCI Capability                 |
| 100h          | AER_CAP    | Advanced Error Reporting (AER) Capability          | PCIe Extended Capability       |
| 148h          | DEV_CAP    | Device Serial Number Capability                    | PCIe Extended Capability       |
| 168h          | ARI_CAP    | Alternative Routing-ID (ARI) Capability            | PCIe Extended Capability       |
| 178h          | SPCIE_CAP  | Secondary PCI Express Capability (Gen3) Capability | PCIe Extended Capability       |
| 198h          | PL16G_CAP  | Physical Layer 16.0 GT/s Capability                | PCIe Extended Capability       |
| 1C0h          | MARGIN_CAP | Margining Extended Capability Header               | PCIe Extended Capability       |
| 1E8h          | SRIOV_CAP  | Single Root I/O Virtualization (SR-IOV) Capability | PCIe Extended Capability       |
| 3A4h          | DLINK_CAP  | Data Link Feature Extended Capability              | PCIe Extended Capability       |

#### 5.1.2 PCI Configuration Header Space Registers Detail

##### 5.1.2.1 PCI Configuration Header Space Registers

[Table 22] PCI Header Space Summary

| Start Address | End Address | Symbol       | Description                                 |
|---------------|-------------|--------------|---------------------------------------------|
| 00h           | 03h         | ID           | Identifiers                                 |
| 04h           | 05h         | CMD          | Command Register                            |
| 06h           | 07h         | STS          | Status Register                             |
| 08h           | 08h         | REVID        | Revision ID                                 |
| 09h           | 0Bh         | CC           | Class Codes                                 |
| 0Ch           | 0Ch         | CLS          | Cache Line Size                             |
| 0Dh           | 0Dh         | MLT          | Master Latency Timer                        |
| 0Eh           | 0Eh         | HTYPE        | Header Type                                 |
| 0Fh           | 0Fh         | BIST         | Built in Self Test                          |
| 10h           | 13h         | MLBAR (BAR0) | Memory Register Base Address (Lower 32-bit) |
| 14h           | 17h         | MUBAR (BAR1) | Memory Register Base Address (Upper 32-bit) |
| 18h           | 1Bh         | IDBAR (BAR2) | Reserved                                    |
| 1Ch           | 1Fh         | BAR3         | Reserved                                    |
| 20h           | 23h         | BAR4         | Reserved                                    |
| 24h           | 27h         | BAR5         | Reserved                                    |
| 28h           | 2Bh         | CCPTR        | CardBus CIS Pointer                         |
| 2Ch           | 2Fh         | SS           | Subsystem Identifiers                       |
| 30h           | 33h         | EXPROM       | Expansion ROM Base Address                  |
| 34h           | 34h         | CAP          | Capabilities Pointer                        |
| 35h           | 3Bh         | R            | Reserved                                    |
| 3Ch           | 3Dh         | INTR         | Interrupt Information                       |
| 3Eh           | 3Eh         | MGNT         | Minimum Grant                               |
| 3Fh           | 3Fh         | MLAT         | Maximum Latency                             |

[Table 23] Identifier Register

| Bits  | Type | Default Value | Description |
|-------|------|---------------|-------------|
| 31:16 | RO   | A824h         | Device ID   |
| 0:15  | RO   | 144Dh         | Vendor ID   |

[Table 24] Command Register

| Bits  | Type | Default Value | Description                               |
|-------|------|---------------|-------------------------------------------|
| 15:11 | RO   | 0             | Reserved                                  |
| 10    | RW   | 0             | Interrupt Disable                         |
| 9     | RO   | 0             | Fast Back-to-Back Enable (N/A)            |
| 8     | RW   | 0             | SERR# Enable                              |
| 7     | RO   | 0             | IDSEL Stepping / Wait Cycle Control (N/A) |
| 6     | RW   | 0             | Parity Error Response Enable              |
| 5     | RO   | 0             | VGA Palette Snooping Enable (N/A)         |
| 4     | RO   | 0             | Memory Write and Invalidate Enable (N/A)  |
| 3     | RO   | 0             | Special Cycle Enable (N/A)                |
| 2     | RW   | 0             | Bus Master Enable                         |
| 1     | RW   | 0             | Memory Space Enable                       |
| 0     | RW   | 0             | I/O Space Enable                          |

[Table 25] Status Register

| Bits | Type | Default Value | Description                                 |
|------|------|---------------|---------------------------------------------|
| 15   | RW1C | 0             | Detected Parity Error                       |
| 14   | RW1C | 0             | Signaled System Error                       |
| 13   | RW1C | 0             | Received Master Abort                       |
| 12   | RW1C | 0             | Received Target Abort                       |
| 11   | RW1C | 0             | Signaled Target Abort (N/A)                 |
| 10:9 | RO   | 0             | DEVSEL Timing (N/A)                         |
| 8    | RW1C | 0             | Master Data Parity Error Detected (N/A)     |
| 7    | RO   | 0             | Fast Back-to-Back Transaction Capable (N/A) |
| 6    | RO   | 0             | Reserved                                    |
| 5    | RO   | 0             | 66MHz Capable (N/A)                         |
| 4    | RO   | 1             | Capabilities List                           |
| 3    | RO   | 0             | Interrupt Status                            |
| 2:1  | RO   | 0             | Reserved                                    |
| 0    | RO   | 0             | Reserved                                    |

[Table 26] Revision ID Register

| Bits | Type | Default Value | Description                     |
|------|------|---------------|---------------------------------|
| 7:0  | RO   | 00h           | Controller Hardware Revision ID |

[Table 27] Class Code Register

| Bits  | Type | Default Value | Description           |
|-------|------|---------------|-----------------------|
| 23:16 | RO   | 01h           | Base Class Code       |
| 15:8  | RO   | 08h           | Sub Class Code        |
| 7:0   | RO   | 02h           | Programming Interface |

[Table 28] Cache Line Size Register

| Bits | Type | Default Value | Description           |
|------|------|---------------|-----------------------|
| 7:0  | RW   | 0             | Cache Line Size (N/A) |

[Table 29] Master Latency Timer Register

| Bits | Type | Default Value | Description                |
|------|------|---------------|----------------------------|
| 7:0  | RO   | 0             | Master Latency Timer (N/A) |

[Table 30] Header Type Register

| Bits | Type | Default Value | Description                 |
|------|------|---------------|-----------------------------|
| 7    | RO   | 0             | Multi-function Device (N/A) |
| 6:0  | RO   | 0             | Reserved                    |

[Table 31] Built In Self Test Register

| Bits | Type | Default Value | Description              |
|------|------|---------------|--------------------------|
| 7    | RO   | 0             | Built In Self Test (N/A) |
| 6    | RO   | 0             | Built In Self Test (N/A) |
| 5:4  | RO   | 0             | Built In Self Test (N/A) |
| 3:0  | RO   | 0             | Built In Self Test (N/A) |

[Table 32] Memory Register Base Address Lower 32-bits (BAR0) Register

| Bits  | Type | Default Value | Description                    |
|-------|------|---------------|--------------------------------|
| 31:15 | RW   | 0             | Base Address                   |
| 14:4  | RO   | 0             | Reserved                       |
| 3     | RO   | 0             | Pre-Fetchable                  |
| 2:1   | RO   | 2h            | Address Type (64-bit)          |
| 0     | RO   | 0             | Memory Space Indicator (MEMSI) |

[Table 33] Memory Register Base Address Upper 32-bits (BAR1)

| Bits | Type | Default Value | Description  |
|------|------|---------------|--------------|
| 31:0 | RW   | 0             | Base Address |

[Table 34] Index/Data Pair Register Base Address (BAR2) Register

| Bits | Type | Default Value | Description |
|------|------|---------------|-------------|
| 31:0 | RO   | 0             | N/A         |

[Table 35] BAR3 Register

| Bits | Type | Default Value | Description |
|------|------|---------------|-------------|
| 31:0 | RO   | 0             | N/A         |

[Table 36] Vendor Specific BAR4 Register

| Bits | Type | Default Value | Description |
|------|------|---------------|-------------|
| 31:0 | RO   | 0             | N/A         |

[Table 37] Vendor Specific BAR5 Register

| Bits | Type | Default Value | Description |
|------|------|---------------|-------------|
| 31:0 | RO   | 0             | N/A         |

[Table 38] Cardbus CIS Pointer Register

| Bits | Type | Default Value | Description |
|------|------|---------------|-------------|
| 31:0 | RO   | 0             | N/A         |

[Table 39] Subsystem Identifier Register

| Bits  | Type | Default Value | Description         |
|-------|------|---------------|---------------------|
| 31:16 | RO   | A801h         | Subsystem ID        |
| 15:0  | RO   | 144Dh         | Subsystem Vendor ID |

[Table 40] Expansion ROM Register

| Bits  | Type | Default Value | Description                  |
|-------|------|---------------|------------------------------|
| 31:17 | RW   | F72Eh         | Expansion ROM Base Address   |
| 16:1  | RO   | 0             | Reserved                     |
| 0     | RW   | 1             | Expansion ROM Enable/Disable |

[Table 41] Capabilities Pointer Register

| Bits | Type | Default Value | Description        |
|------|------|---------------|--------------------|
| 7:0  | RO   | 40h           | Capability Pointer |

[Table 42] Interrupt Information Register

| Bits | Type | Default Value | Description    |
|------|------|---------------|----------------|
| 15:8 | RO   | 01h           | Interrupt Pin  |
| 7:0  | RW   | FFh           | Interrupt Line |

[Table 43] Minimum Grant Register

| Bits | Type | Default Value | Description         |
|------|------|---------------|---------------------|
| 7:0  | RO   | 0             | Minimum Grant (N/A) |

[Table 44] Maximum Latency Register

| Bits | Type | Default Value | Description           |
|------|------|---------------|-----------------------|
| 7:0  | RO   | 0             | Maximum Latency (N/A) |

### 5.1.3 PCI Capability Registers

#### 5.1.3.1 PCI Power Management Capability

[Table 45] PCI Power Management Capability Register Summary

| Start Address | End Address | Symbol        | Description                             |
|---------------|-------------|---------------|-----------------------------------------|
| 40h           | 40h         | PCIPM_ID      | PCI Power Management Capability ID      |
| 41h           | 41h         | NEXTCAP       | Next Capability Pointer                 |
| 42h           | 43h         | PCIPM_CAP     | PC Power Management Capabilities        |
| 44h           | 45h         | PCIPM_CS      | PCI Power Management Control and Status |
| 46h           | 46h         | PCIPM_CSR_BSE | PMCSR_BSE Bridge Extensions             |
| 47h           | 47h         | PCIPM_DATA    | Data                                    |

[Table 46] PCI Power Management Capability ID Register

| Bits | Type | Default Value | Description             |
|------|------|---------------|-------------------------|
| 15:8 | RO   | 70h           | Next Capability Pointer |
| 7:0  | RO   | 1h            | Capability ID           |

[Table 47] PCI Power Management Capability Register

| Bits  | Type  | Default Value | Description                                                                |
|-------|-------|---------------|----------------------------------------------------------------------------|
| 15:11 | RO    | 0             | PME Support (N/A)                                                          |
| 10    | RO    | 0             | D2 Support (N/A)                                                           |
| 9     | RO    | 0             | D1 Support (N/A)                                                           |
| 8:6   | RO    | 0             | AUX current (N/A)                                                          |
| 5     | RO    | 0             | Device Specific Initialization (N/A)                                       |
| 4     | RsvdP | 0             | Reserved                                                                   |
| 3     | RO    | 0             | PME Clock (N/A)                                                            |
| 2:0   | RO    | 3h            | Version<br>(Support for PCIe Power Management Interface Spec revision 1.2) |

[Table 48] PCI Power Management Control and Status Register

| Bits  | Type  | Default Value | Description                  |
|-------|-------|---------------|------------------------------|
| 31:24 | RsvdP | 0             | Data register (N/A)          |
| 23    | RO    | 0             | Bus Power/Clock Enable (N/A) |
| 22    | RO    | 0             | B2, B3 support (N/A)         |
| 21:16 | RsvdP | 0             | Reserved                     |
| 15    | RO    | 0             | PME Status (N/A)             |
| 14:13 | RO    | 0             | Data scale (N/A)             |
| 12:9  | RO    | 0             | Data scale (N/A)             |
| 8     | RWS   | 0             | PME Enable (N/A)             |
| 7:4   | RsvdP | 0             | Reserved                     |
| 3     | RO    | 1             | No Soft Reset                |
| 2     | RsvdP | 0             | Reserved                     |
| 1:0   | RW    | 0             | Power State                  |

## 5.1.3.2 MSI-X Capability

[Table 49] MSI-X Capability Summary

| Start Address | End Address | Symbol   | Description                      |
|---------------|-------------|----------|----------------------------------|
| B0h           | B1h         | MSIX_ID  | MSI-X Capability ID              |
| B2h           | B3h         | MSIX_CAP | MSI-X Message Control            |
| B4h           | B7h         | MSIX_TBL | MSI-X Table Offset and Table BIR |
| B8h           | BBh         | MSIX_PBA | MSI-X PBA Offset and PBA BIR     |

[Table 50] MSI-X Identifier Register

| Bits | Type | Default Value | Description             |
|------|------|---------------|-------------------------|
| 15:8 | RO   | 00h           | Next Capability Pointer |
| 7:0  | RO   | 11h           | Capability ID           |

[Table 51] MSI-X Control Register

| Bits  | Type  | Default Value | Description   |
|-------|-------|---------------|---------------|
| 15    | RW    | 0             | MSI-X Enable  |
| 14    | RW    | 0             | Function Mask |
| 13:11 | RsvdP | 0             | Reserved      |
| 10:0  | RO    | 243h          | Table Size    |

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[Table 52] MSI-X Table Offset Register

| Bits | Type | Default Value | Description  |
|------|------|---------------|--------------|
| 31:3 | RO   | 800h          | Table Offset |
| 2:0  | RO   | 0             | Table BIR    |

[Table 53] MSI-X Pending Bit Array Offset Register

| Bits | Type | Default Value | Description              |
|------|------|---------------|--------------------------|
| 31:3 | RO   | 600h          | Pending Bit Array Offset |
| 2:0  | RO   | 0             | Pending Bit Array BIR    |

### 5.1.3.3 PCI Express Capability

[Table 54] PCI Capability Register Summary

| Start Address | End Address | Symbol     | Description                       |
|---------------|-------------|------------|-----------------------------------|
| 70h           | 71h         | PCIE_ID    | PCI Express Capability ID         |
| 72h           | 73h         | PCIE_CAP   | PCI Express Capabilities          |
| 74h           | 77h         | PCIE_DCAP  | PCI Express Device Capabilities   |
| 78h           | 79h         | PCIE_DC    | PCI Express Device Control        |
| 7Ah           | 7Bh         | PCIE_DS    | PCI Express Device Status         |
| 7Ch           | 7Fh         | PCIE_LCAP  | PCI Express Link Capabilities     |
| 80h           | 81h         | PCIE_LC    | PCI Express Link Control          |
| 82h           | 83h         | PCIE_LS    | PCI Express Link Status           |
| 94h           | 97h         | PCIE_DCAP2 | PCI Express Device Capabilities 2 |
| 98h           | 99h         | PCIE_DC2   | PCI Express Device Control 2      |
| 9Ah           | 9Bh         | PCIE_DS2   | PCI Express Device Status 2       |
| 9Ch           | 9Fh         | PCIE_LCAP2 | PCI Express Link Capabilities 2   |
| A0h           | A1h         | PCIE_LC2   | PCI Express Link Control 2        |
| A2h           | A3h         | PCIE_LS2   | PCI Express Link Status 2         |

[Table 55] PCI Express Capability ID Register

| Bits | Type | Default Value | Description             |
|------|------|---------------|-------------------------|
| 15:8 | RO   | B0h           | Next Capability Pointer |
| 7:0  | RO   | 10h           | Capability ID           |

[Table 56] PCI Express Capabilities Register

| Bits  | Type   | Default Value | Description               |
|-------|--------|---------------|---------------------------|
| 15:14 | RsvdP  | 0             | Reserved                  |
| 13:9  | RO     | 0             | Interrupt Message Number  |
| 8     | HWInit | 0             | Slot Implementation (N/A) |
| 7:4   | RO     | 0             | Device/Port Type          |
| 3:0   | RO     | 2h            | Capability Version        |

[Table 57] PCI Express Device Capabilities Register

| Bits  | Type  | Default Value | Description                     |
|-------|-------|---------------|---------------------------------|
| 31:29 | RsvdP | 0             | Reserved                        |
| 28    | RO    | 1             | Function Level Reset Capability |
| 27:26 | RO    | 0             | Captured Slot Power Limit Scale |
| 25:18 | RO    | 0             | Captured Slot Power Limit Value |
| 17:16 | RsvdP | 0             | Reserved                        |

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|       |    |    |                                |
|-------|----|----|--------------------------------|
| 15    | RO | 1  | Role-based Error Reporting     |
| 14:12 | RO | 0  | Reserved                       |
| 11:9  | RO | 7h | Endpoint L1 Acceptable Latency |
| 8:6   | RO | 7h | Endpoint L0 Acceptable Latency |
| 5     | RO | 1  | Extended Tag Field Supported   |
| 4:3   | RO | 0  | Phantom Functions Supported    |
| 2:0   | RO | 2h | Max Payload Size Supported     |

[Table 58] PCI Express Device Control Register

| Bits  | Type | Default Value | Description                          |
|-------|------|---------------|--------------------------------------|
| 15    | RW   | 0             | Initiate Function Level Reset        |
| 14:12 | RW   | 2h            | Max Read Request Size                |
| 11    | RW   | 1h            | Enable No Snoop                      |
| 10    | RWS  | 0             | Aux Power PM Enable (N/A)            |
| 9     | RW   | 0             | Phantom Functions Enable (N/A)       |
| 8     | RW   | 1h            | Extended Tag Enable                  |
| 7:5   | RW   | 0             | Max Payload Size                     |
| 4     | RW   | 1h            | Enable Relaxed Ordering              |
| 3     | RW   | 0             | Unsupported Request Reporting Enable |
| 2     | RW   | 0             | Fatal Error Reporting Enable         |
| 1     | RW   | 0             | Non-Fatal Error Reporting Enable     |
| 0     | RW   | 0             | Correctable Error Reporting Enable   |

[Table 59] PCI Express Device Status Register

| Bits | Type  | Default Value | Description                  |
|------|-------|---------------|------------------------------|
| 15:6 | RsvdZ | 0             | Reserved                     |
| 5    | RO    | 0             | Transactions Pending         |
| 4    | RO    | 0             | Aux Power Detected           |
| 3    | RW1C  | 0             | Unsupported Request Detected |
| 2    | RW1C  | 0             | Fatal Error Detected         |
| 1    | RW1C  | 0             | Non-Fatal Error Detected     |
| 0    | RW1C  | 0             | Correctable Error Detected   |

[Table 60] PCI Express Link Capabilities Register

| Bits  | Type   | Default Value                                        | Description                                         |
|-------|--------|------------------------------------------------------|-----------------------------------------------------|
| 31:24 | HWInit | 0 (Port 0)                                           | Port Number                                         |
| 23    | RsvdP  | 0                                                    | Reserved                                            |
| 22    | HWInit | 1h                                                   | ASPM Optionality Compliance                         |
| 21    | RO     | 0                                                    | Link Bandwidth Notification Capability (N/A)        |
| 20    | RO     | 0                                                    | Data Link Layer Link Active Reporting Capable (N/A) |
| 19    | RO     | 0                                                    | Surprise Down Error Reporting Capable (N/A)         |
| 18    | RO     | 0                                                    | Clock Power Management                              |
| 17:15 | RO     | 6h                                                   | L1 Exit Latency                                     |
| 14:12 | RO     | 7h                                                   | L0s Exit Latency                                    |
| 11:10 | RO     | 0                                                    | Active State Power Management Support               |
| 9:4   | RO     | Single Port: 4h (x4 link)<br>Dual Port: 2h (x2 link) | Maximum Link Width                                  |
| 3:0   | RO     | 3h                                                   | Max Link Speeds                                     |

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[Table 61] PCI Express Link Control Register

| Bits  | Type     | Default Value | Description                                      |
|-------|----------|---------------|--------------------------------------------------|
| 15:14 | RW/RsvdP | 0             | Reserved                                         |
| 13:12 | RsvdP    | 0             | Reserved                                         |
| 11    | RsvdP    | 0             | Link Autonomous Bandwidth interrupt enable (N/A) |
| 10    | RsvdP    | 0             | Link Bandwidth management interrupt enable (N/A) |
| 9     | RW       | 0             | Hardware Autonomous Width Disable                |
| 8     | RW       | 0             | Enable Clock Power Management                    |
| 7     | RW       | 0             | Extended Sync                                    |
| 6     | RW       | 0             | Common Clock Configuration                       |
| 5     | RsvdP    | 0             | Retrain Link (N/A)                               |
| 4     | RsvdP    | 0             | Link Disable (N/A)                               |
| 3     | RW       | 0             | Read Completion Boundary (N/A)                   |
| 2     | RsvdP    | 0             | Reserved                                         |
| 1:0   | RW       | 0             | Active State Power Management Control            |

[Table 62] PCI Express Link Status Register

| Bits | Type   | Default Value | Description                            |
|------|--------|---------------|----------------------------------------|
| 15   | RsvdP  | 0h            | Link Autonomous Bandwidth Status (N/A) |
| 14   | RsvdP  | 0             | Link Bandwidth Management Status (N/A) |
| 13   | RO     | 0             | Data Link Layer Link Active            |
| 12   | HWInit | 1             | Slot Clock Configuration               |
| 11   | RO     | 0             | Link Training (N/A)                    |
| 10   | RO     | 0             | Reserved                               |
| 9:4  | RO     | 1h            | Negotiated Link Width                  |
| 3:0  | RO     | 0             | Current Link Speed                     |

[Table 63] PCI Express Device Capabilities 2 Register

| Bits  | Type   | Default Value | Description                                |
|-------|--------|---------------|--------------------------------------------|
| 31    | HWInit | 0             | Reserved                                   |
| 30:24 | RsvdP  | 0             | Reserved                                   |
| 23:22 | HWInit | 0             | Max End-End TLP Prefixes (N/A)             |
| 21    | HWInit | 0             | End-End TLP Prefix Supported (N/A)         |
| 20    | RO     | 0             | Extended Format Field Supported (N/A)      |
| 19:18 | HWInit | 0             | OBFF Supported (N/A)                       |
| 17:16 | RsvdP  | 0             | Reserved                                   |
| 15:14 | HWInit | 0             | LN System CLS (N/A)                        |
| 13:12 | RO     | 0             | TPH Completer Supported (N/A)              |
| 11    | RO     | 0             | Latency Tolerance Reporting Supported      |
| 10    | HWInit | 0             | No RO-enabled PR-PR Passing (N/A)          |
| 9     | RO     | 0             | 128-bit CAS Completer Supported (N/A)      |
| 8     | RO     | 0             | 64-bit Atomic Op Completer Supported (N/A) |
| 7     | RO     | 0             | 32-bit Atomic Op Completer Supported (N/A) |
| 6     | RO     | 0             | Atomic Op Routing Supported (N/A)          |
| 5     | RO     | 0             | ARI Forwarding Supported (N/A)             |
| 4     | RO     | 1             | Completion Timeout Disable Supported       |
| 3:0   | HWInit | Fh            | Completion Timeout Ranges Supported        |

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[Table 64] PCI Express Device Control 2 Register

| Bits  | Type     | Default Value | Description                                  |
|-------|----------|---------------|----------------------------------------------|
| 15    | RsvdP    | 0             | End-to-end TLP Prefix Blocking (N/A)         |
| 14:13 | RW/RsvdP | 0             | OBFF Enable (N/A)                            |
| 12:11 | RsvdP    | 0             | Reserved                                     |
| 10    | RW/RsvdP | 0             | Latency Tolerance Reporting Mechanism Enable |
| 9     | RW       | 0             | IDO Completion enable (N/A)                  |
| 8     | RW       | 0             | IDO Request Enable (N/A)                     |
| 7     | RW       | 0             | AtomicOp Egress Blocking (N/A)               |
| 6     | RW       | 0             | AtomicOp Requester Enable (N/A)              |
| 5     | RW       | 0             | ARI forwarding supported (N/A)               |
| 4     | RW       | 0             | Completion Timeout Disable                   |
| 3:0   | RW       | 0             | Completion Timeout Value                     |

[Table 65] PCI Express Device Status 2 Register

| Bits | Type  | Default Value | Description |
|------|-------|---------------|-------------|
| 15:0 | RsvdZ | 0             | Reserved    |

[Table 66] PCI Express Link Capabilities 2 Register

| Bits  | Type   | Default Value | Description                                          |
|-------|--------|---------------|------------------------------------------------------|
| 31    | RO     | 0             | Reserved                                             |
| 30:24 | RsvdP  | 0             | Reserved                                             |
| 23    | HWInit | 0             | Reserved                                             |
| 22:16 | HWInit | 0             | Lower SKP OS Reception Supported Speed Vector (N/A)  |
| 15:9  | HWInit | 0             | Lower SKP OS Generation Supported Speed Vector (N/A) |
| 8     | RO     | 0             | Cross-Link Supported (N/A)                           |
| 7:1   | RO     | 7h            | Supported Link Speeds                                |
| 0     | RsvdP  | 0             | Reserved                                             |

[Table 67] PCI Express Link Control 2 Register

| Bits  | Type      | Default Value | Description                       |
|-------|-----------|---------------|-----------------------------------|
| 15:12 | RWS/RsvdP | 0             | Compliance De-emphasis            |
| 11    | RWS/RsvdP | 0             | Compliance SOS                    |
| 10    | RWS/RsvdP | 0             | Enter Modified Compliance         |
| 9:7   | RWS/RsvdP | 0             | Transmit Margin                   |
| 6     | HWInit    | 0             | Select De-Emphasis (N/A)          |
| 5     | RWS/RsvdP | 0             | Hardware Autonomous Speed Disable |
| 4     | RWS/RsvdP | 0             | Enter Compliance                  |
| 3:0   | RWS/RsvdP | 3h            | Target Link Speed                 |

[Table 68] PCI Express Link Status 2 Register

| Bits | Type  | Default Value | Description                             |
|------|-------|---------------|-----------------------------------------|
| 15:6 | RsvdP | 0             | Reserved                                |
| 5    | RW1CS | 0             | Link Equalization Request 8.0GT/s       |
| 4    | ROS   | 0             | Equalization 8.0GT/s Phase 3 Successful |
| 3    | ROS   | 0             | Equalization 8.0GT/s Phase 2 Successful |
| 2    | ROS   | 0             | Equalization 8.0GT/s Phase 1 Successful |

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|   |     |   |                               |
|---|-----|---|-------------------------------|
| 1 | ROS | 0 | Equalization 8.0GT/s Complete |
| 0 | RO  | 1 | Current De-Emphasis           |

## 5.1.4 PCI Extended Capability Details

## 5.1.4.1 Advanced Error Reporting Registers

[Table 69] Advanced Error Reporting Capability Summary

| Start Address | End Address | Symbol     | Description                                 |
|---------------|-------------|------------|---------------------------------------------|
| 100h          | 103h        | AER_ID     | AER Capability ID                           |
| 104h          | 107h        | AER_UCES   | AER Uncorrectable Error Status              |
| 108h          | 10Bh        | AER_UCEM   | AER Uncorrectable Error Mask                |
| 10Ch          | 10Fh        | AER_UCESEV | AER Uncorrectable Error Severity            |
| 110h          | 113h        | AER_CES    | AER Correctable Error Status                |
| 114h          | 117h        | AER_CEM    | AER Correctable Error Mask                  |
| 118h          | 11Bh        | AER_CC     | AER Advanced Error Capabilities and Control |
| 11Ch          | 12Bh        | AER_HL     | AER Header Log                              |

[Table 70] AER Capability ID Register

| Bits  | Type | Default Value | Description             |
|-------|------|---------------|-------------------------|
| 31:20 | RO   | 148h          | Next Capability Pointer |
| 19:16 | RO   | 2h            | Capability Version      |
| 15:0  | RO   | 1h            | Capability ID           |

[Table 71] AER Uncorrectable Error Status Register

| Bits  | Type      | Default Value | Description                              |
|-------|-----------|---------------|------------------------------------------|
| 31:27 | RsvdZ     | 0             | Reserved                                 |
| 26    | RW1CS     | 0             | Poisoned TLP Egress Blocked Status (N/A) |
| 25    | RW1CS     | 0             | TLP Prefix Blocked Error Status (N/A)    |
| 24    | RW1CS     | 0             | Atomic Op Egress Blocked Status (N/A)    |
| 23    | RW1CS     | 0             | MC Blocked TLP Status (N/A)              |
| 22    | RW1CS     | 0             | Uncorrectable Internal Error Status      |
| 21    | RW1CS     | 0             | ACS Violation Status (N/A)               |
| 20    | RW1CS     | 0             | Unsupported Request Error Status         |
| 19    | RW1CS     | 0             | ECRC Error Status                        |
| 18    | RW1CS     | 0             | Malformed TLP Status                     |
| 17    | RW1CS     | 0             | Receiver Overflow Status                 |
| 16    | RW1CS     | 0             | Unexpected Completion Status             |
| 15    | RW1CS     | 0             | Completer Abort Status                   |
| 14    | RW1CS     | 0             | Completion Timeout Status                |
| 13    | RW1CS     | 0             | Flow Control Protocol Error Status       |
| 12    | RW1CS     | 0             | Poisoned TLP Status                      |
| 11:6  | RsvdZ     | 0             | Reserved                                 |
| 5     | RW1CS     | 0             | Surprise Down Error Status (N/A)         |
| 4     | RW1CS     | 0             | Data Link Protocol Error Status          |
| 3:1   | RsvdZ     | 0             | Reserved                                 |
| 0     | Undefined | 0             | Undefined                                |

[Table 72] AER Uncorrectable Error Mask Register

| Bits  | Type      | Default Value | Description                            |
|-------|-----------|---------------|----------------------------------------|
| 31:27 | RsvdP     | 0             | Reserved                               |
| 26    | RWS       | 0             | Poisoned TLP Egress Blocked Mask (N/A) |
| 25    | RWS       | 0             | TLP Prefix Blocked Error Mask (N/A)    |
| 24    | RWS       | 0             | Atomic Op Egress Blocked Mask (N/A)    |
| 23    | RWS       | 0             | MC Blocked TLP Mask (N/A)              |
| 22    | RWS       | 1             | Uncorrectable Internal Error Mask      |
| 21    | RWS       | 0             | ACS Violation Mask (N/A)               |
| 20    | RWS       | 0             | Unsupported Request Error Mask         |
| 19    | RWS       | 0             | ECRC Error Mask                        |
| 18    | RWS       | 0             | Malformed TLP Mask                     |
| 17    | RWS       | 0             | Receiver Overflow Mask                 |
| 16    | RWS       | 0             | Unexpected Completion Mask             |
| 15    | RWS       | 0             | Completer Abort Mask                   |
| 14    | RWS       | 0             | Completion Timeout Mask                |
| 13    | RWS       | 0             | Flow Control Protocol Error Mask       |
| 12    | RWS       | 0             | Poisoned TLP Mask                      |
| 11:6  | RsvdP     | 0             | Reserved                               |
| 5     | RWS       | 0             | Surprise Down Error Mask (N/A)         |
| 4     | RWS       | 0             | Data Link Protocol Error Mask          |
| 3:1   | RsvdP     | 0             | Reserved                               |
| 0     | Undefined | 0             | Undefined                              |

[Table 73] AER Uncorrectable Error Severity Register

| Bits  | Type      | Default Value | Description                                |
|-------|-----------|---------------|--------------------------------------------|
| 31:27 | RsvdP     | 0             | Reserved                                   |
| 26    | RWS       | 0             | Poisoned TLP Egress Blocked Severity (N/A) |
| 25    | RWS       | 0             | TLP Prefix Blocked Error Severity (N/A)    |
| 24    | RWS       | 0             | Atomic Op Egress Blocked Severity (N/A)    |
| 23    | RWS       | 0             | MC Blocked TLP Severity (N/A)              |
| 22    | RWS       | 1             | Uncorrectable Internal Error Severity      |
| 21    | RWS       | 0             | ACS Violation Severity (N/A)               |
| 20    | RWS       | 0             | Unsupported Request Error Severity         |
| 19    | RWS       | 0             | ECRC Error Severity                        |
| 18    | RWS       | 1             | Malformed TLP Severity                     |
| 17    | RWS       | 1             | Receiver Overflow Severity                 |
| 16    | RWS       | 0             | Unexpected Completion Severity             |
| 15    | RWS       | 0             | Completer Abort Severity                   |
| 14    | RWS       | 0             | Completion Timeout Severity                |
| 13    | RWS       | 1             | Flow Control Protocol Error Severity       |
| 12    | RWS       | 0             | Poisoned TLP Severity                      |
| 11:6  | RsvdP     | 0             | Reserved                                   |
| 5     | RWS       | 1             | Surprise Down Error Severity (N/A)         |
| 4     | RWS       | 1             | Data Link Protocol Error Severity          |
| 3:1   | RsvdP     | 0             | Reserved                                   |
| 0     | Undefined | 0             | Undefined                                  |

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[Table 74] AER Correctable Error Status Register

| Bits  | Type  | Default Value | Description                     |
|-------|-------|---------------|---------------------------------|
| 31:16 | RsvdZ | 0             | Reserved                        |
| 15    | RW1CS | 0             | Header Log Overflow Status      |
| 14    | RW1CS | 0             | Corrected Internal Error Status |
| 13    | RW1CS | 0             | Advisory Non-Fatal Error Status |
| 12    | RW1CS | 0             | Replay Timer Timeout Status     |
| 11:9  | RsvdZ | 0             | Reserved                        |
| 8     | RW1CS | 0             | Replay Number Rollover Status   |
| 7     | RW1CS | 0             | Bad DLLP Status                 |
| 6     | RW1CS | 0             | Bad TLP Status                  |
| 5:1   | RsvdZ | 0             | Reserved                        |
| 0     | RW1CS | 0             | Received Error Status           |

[Table 75] AER Correctable Error Mask Register

| Bits  | Type  | Default Value | Description                   |
|-------|-------|---------------|-------------------------------|
| 31:16 | RsvdP | 0             | Reserved                      |
| 15    | RWS   | 1             | Header Log Overflow Mask      |
| 14    | RWS   | 1             | Corrected Internal Error Mask |
| 13    | RWS   | 1             | Advisory Non-Fatal Error Mask |
| 12    | RWS   | 0             | Replay Timer Timeout Mask     |
| 11:9  | RsvdP | 0             | Reserved                      |
| 8     | RWS   | 0             | Replay Number Rollover Mask   |
| 7     | RWS   | 0             | Bad DLLP Mask                 |
| 6     | RWS   | 0             | Bad TLP Mask                  |
| 5:1   | RsvdP | 0             | Reserved                      |
| 0     | RWS   | 0             | Received Error Mask           |

[Table 76] AER Capabilities and Control Register

| Bits  | Type  | Default Value | Description                                        |
|-------|-------|---------------|----------------------------------------------------|
| 31:13 | RsvdP | 0             | Reserved                                           |
| 12    | RO    | 0             | Completion Timeout Prefix/Header Log Capable (N/A) |
| 11    | ROS   | 0             | TLP Prefix Log Present (N/A)                       |
| 10    | RWS   | 0             | Multiple Header Recording Enable                   |
| 9     | RO    | 1             | Multiple Header Recording Capable                  |
| 8     | RWS   | 0             | ECRC Check Enable                                  |
| 7     | RO    | 1             | ECRC Check Capable                                 |
| 6     | RWS   | 0             | ECRC Generation Enable                             |
| 5     | RO    | 1             | ECRC Generation Capable                            |
| 4:0   | ROS   | 0             | First Error Pointer                                |

[Table 77] AER Header Log Register

| Bits    | Type | Default Value | Description   |
|---------|------|---------------|---------------|
| 127:120 | ROS  | 0             | Header Byte 0 |
| 119:112 | ROS  | 0             | Header Byte 1 |
| 111:104 | ROS  | 0             | Header Byte 2 |
| 103:96  | ROS  | 0             | Header Byte 3 |

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|       |     |   |                |
|-------|-----|---|----------------|
| 95:88 | ROS | 0 | Header Byte 4  |
| 87:80 | ROS | 0 | Header Byte 5  |
| 79:72 | ROS | 0 | Header Byte 6  |
| 71:64 | ROS | 0 | Header Byte 7  |
| 63:56 | ROS | 0 | Header Byte 8  |
| 55:48 | ROS | 0 | Header Byte 9  |
| 47:40 | ROS | 0 | Header Byte 10 |
| 39:32 | ROS | 0 | Header Byte 11 |
| 31:24 | ROS | 0 | Header Byte 12 |
| 23:16 | ROS | 0 | Header Byte 13 |
| 15:8  | ROS | 0 | Header Byte 14 |
| 7:0   | ROS | 0 | Header Byte 15 |

#### 5.1.4.2 Device serial number capability registers

[Table 78] Device serial number capability Summary

| Start Address | End Address | Symbol | Description                                     |
|---------------|-------------|--------|-------------------------------------------------|
| 148h          | 14Bh        |        | Device Serial Number Extended Capability Header |
| 14Ch          | 14Fh        |        | Serial Number Register (Lower DW)               |
| 150h          | 153h        |        | Serial Number Register (Upper DW)               |

[Table 79] Device Serial Number Extended Capability Header

| Bits  | Type   | Default Value | Description                                                             |
|-------|--------|---------------|-------------------------------------------------------------------------|
| 31:20 | RO     | 168h          | Next Capability Pointer                                                 |
| 19:16 | Hwlnit | 1h            | Capability Version                                                      |
| 15:0  | Hwlnit | 3h            | Serial number capability ID (Secondary PCI Express Extended capability) |

[Table 80] Device Serial Number Register (Upper and Lower DW)

| Bits | Type | Default Value | Description                   |
|------|------|---------------|-------------------------------|
| 31:0 | RO   | Serial Number | Device serial number register |

#### 5.1.4.3 Alternative Routing-ID(ARI) Capability

[Table 81] Alternative Routing-ID(ARI) Capability Summary

| Start Address | End Address | Symbol        | Description                                   |
|---------------|-------------|---------------|-----------------------------------------------|
| 168h          | 16Bh        | Serial Number | Alternative Routing-ID(ARI) Capability Header |
| 16Ch          | 16Dh        |               | ARI Capability Register                       |
| 16Eh          | 16Fh        |               | ARI Control Register                          |

[Table 82] Alternative Routing-ID(ARI) Capability Header

| Bits  | Type | Default Value | Description                        |
|-------|------|---------------|------------------------------------|
| 31:20 | RO   | 178h          | Next Capability Pointer            |
| 19:16 | RO   | 1h            | Capability Version                 |
| 15:0  | RO   | Eh            | PCI Express Extended Capability ID |

[Table 83] ARI Capability Register

| Bits | Type | Default Value | Description                     |
|------|------|---------------|---------------------------------|
| 15:8 | RO   | 0             | Next Function Number            |
| 7:2  | RO   | 0             | RsvdP                           |
| 1    | RO   | 0             | ACS Function Groups Capability  |
| 0    | RO   | 0             | MFVC Function Groups Capability |

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[Table 84] ARI Control Register

| Bits | Type  | Default Value | Description                 |
|------|-------|---------------|-----------------------------|
| 15:7 | RsvdP | 0             | RsvdP                       |
| 6:4  | RW    | 0             | Function Group              |
| 3:2  | RsvdP | 0             | RsvdP                       |
| 1    | RW    | 0             | ACS Function Groups Enable  |
| 0    | RW    | 0             | MFVC Function Groups Enable |

#### 5.1.4.4 Secondary PCI Express Capability

[Table 85] Secondary PCI Express Capability Summary

| Start Address | End Address | Symbol   | Description                             |
|---------------|-------------|----------|-----------------------------------------|
| 178h          | 17Bh        | SPE_ID   | Secondary PCI Express Capability        |
| 17Ch          | 17Fh        | SPE_LC3  | PCI Express Link Control 3              |
| 180h          | 183h        | SPE_LE   | PCI Express Lane Error Status           |
| 184h          | 185h        | SPE_L0EC | PCI Express Lane 0 Equalization Control |
| 186h          | 187h        | SPE_L1EC | PCI Express Lane 1 Equalization Control |
| 188h          | 189h        | SPE_L2EC | PCI Express Lane 2 Equalization Control |
| 18Ah          | 18Bh        | SPE_L3EC | PCI Express Lane 3 Equalization Control |

[Table 86] Secondary PCI Express Capability ID Register

| Bits  | Type | Default Value | Description                                               |
|-------|------|---------------|-----------------------------------------------------------|
| 31:20 | RO   | 000h          | Next Capability offset                                    |
| 19:16 | RO   | 1h            | Capability Version                                        |
| 15:0  | RO   | 19h           | Capability ID (Secondary PCI Express Extended capability) |

[Table 87] PCI Express Link Control 3 Register

| Bits  | Type  | Default Value | Description                                      |
|-------|-------|---------------|--------------------------------------------------|
| 31:16 | RsvdP | 0             | Reserved                                         |
| 15:9  | RW    | 0             | Enable Lower SKP OS Generation Vector (N/A)      |
| 8:2   | RsvdP | 0             | Reserved                                         |
| 1     | RW    | 0             | Link Equalization Request Interrupt Enable (N/A) |
| 0     | RW    | 0             | Perform Equalization (N/A)                       |

[Table 88] PCI Express Lane Error Status Register

| Bits | Type  | Default Value | Description            |
|------|-------|---------------|------------------------|
| 31:4 | RsvdP | 0             | Reserved               |
| 3:0  | RW1CS | 0             | Lane Error Status Bits |

[Table 89] Lane 0 Equalization Control Register

| Bits  | Type         | Default Value | Description                                       |
|-------|--------------|---------------|---------------------------------------------------|
| 15    | RsvdP        | 0             | Reserved                                          |
| 14:12 | HWInit/RO    | 7h            | Upstream Port 8.0T/s Receiver Preset Hint         |
| 11:8  | HWInit/RO    | Fh            | Upstream Port 8.0T/s Transmitter Preset           |
| 7     | RsvdZ        | 0             | Reserved                                          |
| 6:4   | HWInit/RsvdP | 0             | Downstream Port 8.0T/s Receiver Preset Hint (N/A) |
| 3:0   | HWInit/RsvdP | 0             | Downstream Port 8.0T/s Transmitter Preset (N/A)   |

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[Table 90] Lane 1 Equalization Control Register

| Bits  | Type         | Default Value | Description                                       |
|-------|--------------|---------------|---------------------------------------------------|
| 15    | RsvdP        | 0             | Reserved                                          |
| 14:12 | HWInit/RO    | 7h            | Upstream Port 8.0T/s Receiver Preset Hint         |
| 11:8  | HWInit/RO    | Fh            | Upstream Port 8.0T/s Transmitter Preset           |
| 7     | RsvdZ        | 0             | Reserved                                          |
| 6:4   | HWInit/RsvdP | 0             | Downstream Port 8.0T/s Receiver Preset Hint (N/A) |
| 3:0   | HWInit/RsvdP | 0             | Downstream Port 8.0T/s Transmitter Preset (N/A)   |

[Table 91] Lane 2 Equalization Control Register

| Bits  | Type         | Default Value | Description                                       |
|-------|--------------|---------------|---------------------------------------------------|
| 15    | RsvdP        | 0             | Reserved                                          |
| 14:12 | HWInit/RO    | 7h            | Upstream Port 8.0T/s Receiver Preset Hint         |
| 11:8  | HWInit/RO    | Fh            | Upstream Port 8.0T/s Transmitter Preset           |
| 7     | RsvdZ        | 0             | Reserved                                          |
| 6:4   | HWInit/RsvdP | 0             | Downstream Port 8.0T/s Receiver Preset Hint (N/A) |
| 3:0   | HWInit/RsvdP | 0             | Downstream Port 8.0T/s Transmitter Preset (N/A)   |

[Table 92] Lane 3 Equalization Control Register

| Bits  | Type         | Default Value | Description                                       |
|-------|--------------|---------------|---------------------------------------------------|
| 15    | RsvdP        | 0             | Reserved                                          |
| 14:12 | HWInit/RO    | 7h            | Upstream Port 8.0T/s Receiver Preset Hint         |
| 11:8  | HWInit/RO    | Fh            | Upstream Port 8.0T/s Transmitter Preset           |
| 7     | RsvdZ        | 0             | Reserved                                          |
| 6:4   | HWInit/RsvdP | 0             | Downstream Port 8.0T/s Receiver Preset Hint (N/A) |
| 3:0   | HWInit/RsvdP | 0             | Downstream Port 8.0T/s Transmitter Preset (N/A)   |

#### 5.1.4.5 Physical Layer 16.0 GT/s Capability

[Table 93] Physical Layer 16.0 GT/s Capability Summary

| Start Address | End Address | Symbol | Description                                                   |
|---------------|-------------|--------|---------------------------------------------------------------|
| 198h          | 19Bh        |        | Physical Layer 16.0 GT/s Extended Capability Header           |
| 19Ch          | 19Fh        |        | 16.0 GT/s Capabilities Register                               |
| 1A0h          | 1A3h        |        | 16.0 GT/s Control Register                                    |
| 1A4h          | 1A7h        |        | 16.0 GT/s Status Register                                     |
| 1A8h          | 1ABh        |        | 16.0 GT/s Local Data Parity Mismatch Status Register          |
| 1ACh          | 1AFh        |        | 16.0 GT/s First Retimer Data Parity Mismatch Status Register  |
| 1B0h          | 1B3h        |        | 16.0 GT/s Second Retimer Data Parity Mismatch Status Register |
| 1B4h          | 1B7h        |        | Reserved                                                      |
| 1B8h          | 1BBh        |        | 16.0 GT/s Control Register for Lane 0-3                       |
| 1BCh          | 1BFh        |        | 16.0 GT/s Control Register for Lane 4-7                       |

[Table 94] Physical Layer 16.0 GT/s Extended Capability Header

| Bits  | Type | Default Value | Description                                               |
|-------|------|---------------|-----------------------------------------------------------|
| 31:20 | RO   | 1C0h          | Next Capability Pointer                                   |
| 19:16 | RO   | 1h            | Capability Version                                        |
| 15:0  | RO   | 26h           | Capability ID (Secondary PCI Express Extended capability) |

[Table 95] 16.0 GT/s Capabilities Register

| Bits | Type | Default Value | Description |
|------|------|---------------|-------------|
|------|------|---------------|-------------|

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|      |       |   |          |
|------|-------|---|----------|
| 31:0 | RsvdP | 0 | Reserved |
|------|-------|---|----------|

[Table 96] 16.0 GT/s Control Register

| Bits | Type  | Default Value | Description |
|------|-------|---------------|-------------|
| 31:0 | RsvdP | 0             | Reserved    |

[Table 97] 16.0 GT/s Status Register

| Bits | Type        | Default Value | Description                               |
|------|-------------|---------------|-------------------------------------------|
| 31:5 | RsvdZ       | 0             | Reserved                                  |
| 4    | RW1CS/RsvdZ | 0             | Link Equalization Request 16.0 GT/s       |
| 3    | ROS/RsvdZ   | 0             | Equalization 16.0 GT/s Phase 3 Successful |
| 2    | ROS/RsvdZ   | 0             | Equalization 16.0 GT/s Phase 2 Successful |
| 1    | ROS/RsvdZ   | 0             | Equalization 16.0 GT/s Phase 1 Successful |
| 0    | ROS/RsvdZ   | 0             | Equalization 16.0 GT/s Complete           |

[Table 98] 16.0 GT/s Local Data Parity Mismatch Status Register

| Bits | Type  | Default Value | Description                       |
|------|-------|---------------|-----------------------------------|
| 31:8 | RsvdP | 0             | Reserved                          |
| 7:0  | RW1CS | 0             | Local Data Parity Mismatch Status |

[Table 99] 16.0 GT/s First Retimer Data Parity Mismatch Status Register

| Bits | Type  | Default Value | Description                               |
|------|-------|---------------|-------------------------------------------|
| 31:8 | RsvdP | 0             | Reserved                                  |
| 7:0  | RW1CS | 0             | First Retimer Data Parity Mismatch Status |

[Table 100] 16.0 GT/s Second Retimer Data Parity Mismatch Status Register

| Bits | Type  | Default Value | Description                                |
|------|-------|---------------|--------------------------------------------|
| 31:8 | RsvdP | 0             | Reserved                                   |
| 7:0  | RW1CS | 0             | Second Retimer Data Parity Mismatch Status |

[Table 101] Reserved

| Bits | Type  | Default Value | Description |
|------|-------|---------------|-------------|
| 31:0 | RsvdP | 0             | Reserved    |

[Table 102] 16.0 GT/s Control Register for Lane 0-3

| Bits  | Type         | Default Value | Description                                           |
|-------|--------------|---------------|-------------------------------------------------------|
| 31:28 | HwInit/RO    | Fh            | Upstream Port 16.0 GT/s Transmitter Preset (Lane 3)   |
| 27:24 | HwInit/RsvdP | 0h            | Downstream Port 16.0 GT/s Transmitter Preset (Lane 3) |
| 23:20 | HwInit/RO    | Fh            | Upstream Port 16.0 GT/s Transmitter Preset (Lane 2)   |
| 19:16 | HwInit/RsvdP | 0h            | Downstream Port 16.0 GT/s Transmitter Preset (Lane 2) |
| 15:12 | HwInit/RO    | Fh            | Upstream Port 16.0 GT/s Transmitter Preset (Lane 1)   |
| 11:8  | HwInit/RsvdP | 0h            | Downstream Port 16.0 GT/s Transmitter Preset (Lane 1) |
| 7:4   | HwInit/RO    | Fh            | Upstream Port 16.0 GT/s Transmitter Preset (Lane 0)   |
| 3:0   | HwInit/RsvdP | 0h            | Downstream Port 16.0 GT/s Transmitter Preset (Lane 0) |

[Table 103] 16.0 GT/s Control Register for Lane 4-7

| Bits  | Type         | Default Value | Description                                           |
|-------|--------------|---------------|-------------------------------------------------------|
| 31:28 | HwInit/RO    | Fh            | Upstream Port 16.0 GT/s Transmitter Preset (Lane 7)   |
| 27:24 | HwInit/RsvdP | 0h            | Downstream Port 16.0 GT/s Transmitter Preset (Lane 7) |
| 23:20 | HwInit/RO    | Fh            | Upstream Port 16.0 GT/s Transmitter Preset (Lane 6)   |
| 19:16 | HwInit/RsvdP | 0h            | Downstream Port 16.0 GT/s Transmitter Preset (Lane 6) |
| 15:12 | HwInit/RO    | Fh            | Upstream Port 16.0 GT/s Transmitter Preset (Lane 5)   |

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|      |              |    |                                                       |
|------|--------------|----|-------------------------------------------------------|
| 11:8 | HwInit/RsvdP | 0h | Downstream Port 16.0 GT/s Transmitter Preset (Lane 5) |
| 7:4  | HwInit/RO    | Fh | Upstream Port 16.0 GT/s Transmitter Preset (Lane 4)   |
| 3:0  | HwInit/RsvdP | 0h | Downstream Port 16.0 GT/s Transmitter Preset (Lane 4) |

#### 5.1.4.6 Margining Extended Capability Header

[Table 104] Margining Extended Capability Header Summary

| Start Address | End Address | Symbol | Description                              |
|---------------|-------------|--------|------------------------------------------|
| 1C0h          | 1C3h        |        | Margining Extended Capability Header     |
| 1C4h          | 1C5h        |        | Margining Port Capabilities Register     |
| 1C6h          | 1C7h        |        | Margining Port Status Register           |
| 1C8h          | 1C9h        |        | Margining Lane Control Register (Lane 0) |
| 1CAh          | 1CBh        |        | Margining Lane Control Register (Lane 0) |
| 1CCh          | 1CDh        |        | Margining Lane Control Register (Lane 1) |
| 1CEh          | 1CFh        |        | Margining Lane Control Register (Lane 1) |
| 1D0h          | 1D1h        |        | Margining Lane Control Register (Lane 2) |
| 1D2h          | 1D3h        |        | Margining Lane Control Register (Lane 2) |
| 1D4h          | 1D5h        |        | Margining Lane Control Register (Lane 3) |
| 1D6h          | 1D7h        |        | Margining Lane Control Register (Lane 3) |
| 1D8h          | 1D9h        |        | Margining Lane Control Register (Lane 4) |
| 1DAh          | 1DBh        |        | Margining Lane Control Register (Lane 4) |
| 1DCh          | 1DDh        |        | Margining Lane Control Register (Lane 5) |
| 1DEh          | 1DFh        |        | Margining Lane Control Register (Lane 5) |
| 1E0h          | 1E1h        |        | Margining Lane Control Register (Lane 6) |
| 1E2h          | 1E3h        |        | Margining Lane Control Register (Lane 6) |
| 1E4h          | 1E5h        |        | Margining Lane Control Register (Lane 7) |
| 1E6h          | 1E7h        |        | Margining Lane Control Register (Lane 7) |

[Table 105] Physical Layer 16.0 GT/s Margining Capability

| Bits  | Type | Default Value | Description                        |
|-------|------|---------------|------------------------------------|
| 31:20 | RO   | 1E8h          | Next Capability Pointer            |
| 19:16 | RO   | 1h            | Capability Version                 |
| 15:0  | RO   | 27h           | PCI Express Extended Capability ID |

[Table 106] Margining Port Capabilities Register

| Bits | Type   | Default Value | Description                    |
|------|--------|---------------|--------------------------------|
| 15:1 | RsvdP  | 0             | Reserved                       |
| 0    | HWInit | 0             | Margining uses Driver Software |

[Table 107] Margining Port Status Register

| Bits | Type  | Default Value | Description              |
|------|-------|---------------|--------------------------|
| 15:2 | RsvdZ | 0             | Reserved                 |
| 1    | RO    | 0             | Margining Software Ready |
| 0    | RO    | 0             | Margining Ready          |

[Table 108] Margining Lane Control Register (Lane 0)

| Bits | Type  | Default Value | Description    |
|------|-------|---------------|----------------|
| 15:8 | RW    | 9Ch           | Margin Payload |
| 7    | RsvdP | 0             | Reserved       |
| 6    | RW    | 0             | Usage Model    |
| 5:3  | RW    | 7h            | Margin Type    |

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|     |    |   |                 |
|-----|----|---|-----------------|
| 2:0 | RW | 0 | Receiver Number |
|-----|----|---|-----------------|

[Table 109] Margining Lane Status Register (Lane 0)

| Bits | Type  | Default Value | Description            |
|------|-------|---------------|------------------------|
| 15:8 | RO    | 0             | MarginPayload Status   |
| 7    | RsvdP | 0             | Reserved               |
| 6    | RO    | 0             | Usage Model Status     |
| 5:3  | RO    | 0             | Margin Type Status     |
| 2:0  | RO    | 0             | Receiver Number Status |

[Table 110] Margining Lane Control Register (Lane 1)

| Bits | Type  | Default Value | Description     |
|------|-------|---------------|-----------------|
| 15:8 | RW    | 9Ch           | Margin Payload  |
| 7    | RsvdP | 0             | Reserved        |
| 6    | RW    | 0             | Usage Model     |
| 5:3  | RW    | 7h            | Margin Type     |
| 2:0  | RW    | 0             | Receiver Number |

[Table 111] Margining Lane Status Register (Lane 1)

| Bits | Type  | Default Value | Description            |
|------|-------|---------------|------------------------|
| 15:8 | RO    | 0             | MarginPayload Status   |
| 7    | RsvdP | 0             | Reserved               |
| 6    | RO    | 0             | Usage Model Status     |
| 5:3  | RO    | 0             | Margin Type Status     |
| 2:0  | RO    | 0             | Receiver Number Status |

[Table 112] Margining Lane Control Register (Lane 2)

| Bits | Type  | Default Value | Description     |
|------|-------|---------------|-----------------|
| 15:8 | RW    | 9Ch           | Margin Payload  |
| 7    | RsvdP | 0             | Reserved        |
| 6    | RW    | 0             | Usage Model     |
| 5:3  | RW    | 7h            | Margin Type     |
| 2:0  | RW    | 0             | Receiver Number |

[Table 113] Margining Lane Status Register (Lane 2)

| Bits | Type  | Default Value | Description            |
|------|-------|---------------|------------------------|
| 15:8 | RO    | 0             | MarginPayload Status   |
| 7    | RsvdP | 0             | Reserved               |
| 6    | RO    | 0             | Usage Model Status     |
| 5:3  | RO    | 0             | Margin Type Status     |
| 2:0  | RO    | 0             | Receiver Number Status |

[Table 114] Margining Lane Control Register (Lane 3)

| Bits | Type  | Default Value | Description     |
|------|-------|---------------|-----------------|
| 15:8 | RW    | 9Ch           | Margin Payload  |
| 7    | RsvdP | 0             | Reserved        |
| 6    | RW    | 0             | Usage Model     |
| 5:3  | RW    | 7h            | Margin Type     |
| 2:0  | RW    | 0             | Receiver Number |

[Table 115] Margining Lane Status Register (Lane 3)

| Bits | Type  | Default Value | Description     |
|------|-------|---------------|-----------------|
| 15:8 | RW    | 9Ch           | Margin Payload  |
| 7    | RsvdP | 0             | Reserved        |
| 6    | RW    | 0             | Usage Model     |
| 5:3  | RW    | 7h            | Margin Type     |
| 2:0  | RW    | 0             | Receiver Number |

[Table 116] Margining Lane Control Register (Lane 4)

| Bits | Type  | Default Value | Description     |
|------|-------|---------------|-----------------|
| 15:8 | RW    | 9Ch           | Margin Payload  |
| 7    | RsvdP | 0             | Reserved        |
| 6    | RW    | 0             | Usage Model     |
| 5:3  | RW    | 7h            | Margin Type     |
| 2:0  | RW    | 0             | Receiver Number |

[Table 117] Margining Lane Status Register (Lane 4)

| Bits | Type  | Default Value | Description     |
|------|-------|---------------|-----------------|
| 15:8 | RW    | 9Ch           | Margin Payload  |
| 7    | RsvdP | 0             | Reserved        |
| 6    | RW    | 0             | Usage Model     |
| 5:3  | RW    | 7h            | Margin Type     |
| 2:0  | RW    | 0             | Receiver Number |

[Table 118] Margining Lane Control Register (Lane 5)

| Bits | Type  | Default Value | Description     |
|------|-------|---------------|-----------------|
| 15:8 | RW    | 9Ch           | Margin Payload  |
| 7    | RsvdP | 0             | Reserved        |
| 6    | RW    | 0             | Usage Model     |
| 5:3  | RW    | 7h            | Margin Type     |
| 2:0  | RW    | 0             | Receiver Number |

[Table 119] Margining Lane Status Register (Lane 5)

| Bits | Type  | Default Value | Description     |
|------|-------|---------------|-----------------|
| 15:8 | RW    | 9Ch           | Margin Payload  |
| 7    | RsvdP | 0             | Reserved        |
| 6    | RW    | 0             | Usage Model     |
| 5:3  | RW    | 7h            | Margin Type     |
| 2:0  | RW    | 0             | Receiver Number |

[Table 120] Margining Lane Status Register (Lane 6)

| Bits | Spec Type | Default Value | Description            |
|------|-----------|---------------|------------------------|
| 15:8 | RO        | 0             | MarginPayload Status   |
| 7    | RsvdP     | 0             | Reserved               |
| 6    | RO        | 0             | Usage Model Status     |
| 5:3  | RO        | 0             | Margin Type Status     |
| 2:0  | RO        | 0             | Receiver Number Status |

[Table 121] Margining Lane Control Register (Lane 7)

| Bits | Spec Type | Default Value | Description    |
|------|-----------|---------------|----------------|
| 15:8 | RW        | 9Ch           | Margin Payload |

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|     |       |    |                 |
|-----|-------|----|-----------------|
| 7   | RsvdP | 0  | Reserved        |
| 6   | RW    | 0  | Usage Model     |
| 5:3 | RW    | 7h | Margin Type     |
| 2:0 | RW    | 0  | Receiver Number |

[Table 122] Margining Lane Status Register (Lane 7)

| Bits | Spec Type | Default Value | Description            |
|------|-----------|---------------|------------------------|
| 15:8 | RO        | 0             | Margin Payload Status  |
| 7    | RsvdP     | 0             | Reserved               |
| 6    | RO        | 0             | Usage Model Status     |
| 5:3  | RO        | 0             | Margin Type Status     |
| 2:0  | RO        | 0             | Receiver Number Status |

## 5.1.4.7 Single Root I/O Virtualization (SR-IOV) Capability

[Table 123] SR-IOV Extended Capability Header Summary

| Start Address | End Address | Symbol | Description                       |
|---------------|-------------|--------|-----------------------------------|
| 1E8h          | 1EBh        |        | SR-IOV Extended Capability Header |
| 1ECh          | 1EFh        |        | SR-IOV Capabilities               |
| 1F0h          | 1F1h        |        | SR-IOV Control                    |
| 1F2h          | 1F3h        |        | SR-IOV Status                     |
| 1F4h          | 1F5h        |        | InitialVFs                        |
| 1F6h          | 1F7h        |        | TotalVFs                          |
| 1F8h          | 1F9h        |        | NumVFs                            |
| 1FAh          | 1FBh        |        | Function Dependency Link          |
| 1FCh          | 1FDh        |        | First VF Offset                   |
| 1FEh          | 1FFh        |        | VF Stride                         |
| 200h          | 203h        |        | VF Device ID                      |
| 204h          | 207h        |        | Supported Page Sizes              |
| 208h          | 20Bh        |        | System Page Size                  |
| 20Ch          | 20Fh        |        | VF BAR0                           |
| 210h          | 213h        |        | VF BAR1                           |
| 214h          | 217h        |        | VF BAR2                           |
| 218h          | 21Bh        |        | VF BAR3                           |
| 21Ch          | 21Fh        |        | VF BAR4                           |
| 220h          | 223h        |        | VF BAR5                           |
| 224h          | 227h        |        | VF Migration State Array Offset   |

[Table 124] SR-IOV Extended Capability Header

| Bits  | Spec Type | Default Value | Description                        |
|-------|-----------|---------------|------------------------------------|
| 31:20 | RO        | 3A4h          | Next Capability Offset (End)       |
| 19:16 | RO        | 1h            | Capability Version                 |
| 15:0  | RO        | 0010h         | PCI Express Extended Capability ID |

[Table 125] SR-IOV Capabilities

| Bits  | Spec Type | Default Value | Description                           |
|-------|-----------|---------------|---------------------------------------|
| 31:21 | RO        | 0h            | VF Migration Interrupt Message Number |
| 20:3  | RsvdP     | 0h            | Reserved                              |

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|   |        |    |                                   |
|---|--------|----|-----------------------------------|
| 2 | HwInit | 0h | VF 10-Bit Tag Requester Supported |
| 1 | RO     | 1h | ARI Capable Hierarchy Preserved   |
| 0 | RO     | 0h | VF Migration Capable              |

[Table 126] SR-IOV Control

| Bits | Spec Type | Default Value | Description                    |
|------|-----------|---------------|--------------------------------|
| 15:6 | RsvdP     | 0h            | Reserved                       |
| 5    | RW or RO  | 0             | VF 10-Bit Tag Requester Enable |
| 4    | RW or RO  | 0             | ARI Capable Hierarchy          |
| 3    | RW        | 0             | VF MSE                         |
| 2    | RW        | 0             | VF Migration Interrupt Enable  |
| 1    | RW or RO  | 0             | VF Migration Enable            |
| 0    | RW        | 0             | VF Enable                      |

[Table 127] SR-IOV Status

| Bits | Spec Type | Default Value | Description         |
|------|-----------|---------------|---------------------|
| 15:1 | RsvdZ     | 0h            | Reserved            |
| 0    | RW1C      | 0             | VF Migration Status |

[Table 128] InitialVFs

| Bits | Spec Type | Default Value | Description |
|------|-----------|---------------|-------------|
| 15:0 | HwInit/RO | 40h           | InitialVFs  |

[Table 129] TotalVFs

| Bits | Spec Type | Default Value | Description |
|------|-----------|---------------|-------------|
| 15:0 | HwInit/RO | 40h           | TotalVFs    |

[Table 130] NumVFs

| Bits | Spec Type | Default Value | Description |
|------|-----------|---------------|-------------|
| 15:0 | RW        | 0h            | NumVFs      |

[Table 131] Function Dependency Link

| Bits | Spec Type | Default Value | Description              |
|------|-----------|---------------|--------------------------|
| 15:8 |           | 0h            | Reserved                 |
| 7:0  |           | 0h            | Function Dependency Link |

[Table 132] First VF Offset

| Bits | Spec Type | Default Value | Description     |
|------|-----------|---------------|-----------------|
| 15:0 | RO        | 2h            | First VF Offset |

[Table 133] VF Stride

| Bits | Spec Type | Default Value | Description |
|------|-----------|---------------|-------------|
| 15:0 | RO        | 1h            | VF Stride   |

[Table 134] VF Device ID

| Bits  | Spec Type | Default Value | Description  |
|-------|-----------|---------------|--------------|
| 31:16 | RO        | A824h         | VF Device ID |
| 15:0  | RsvdP     | 0h            | Reserved     |

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[Table 135] Supported Page Sizes

| Bits | Spec Type | Default Value | Description          |
|------|-----------|---------------|----------------------|
| 31:0 | RO        | 553h          | Supported Page Sizes |

[Table 136] System Page Size

| Bits | Spec Type | Default Value | Description      |
|------|-----------|---------------|------------------|
| 31:0 | RW        | 1h            | System Page Size |

[Table 137] VF BAR0

| Bits  | Spec Type | Default Value | Description                    |
|-------|-----------|---------------|--------------------------------|
| 31:15 |           | 0             | VF Base Address                |
| 14:4  |           | 0             | Reserved                       |
| 3     |           | 0             | Pre-Fetchable                  |
| 2:1   |           | 2h            | Address Type (64-bit)          |
| 0     | RO        | 0             | Memory Space Indicator (MEMSI) |

[Table 138] VF BAR1

| Bits | Spec Type | Default Value | Description |
|------|-----------|---------------|-------------|
| 31:0 |           | 0h            | VF BAR1     |

[Table 139] VF BAR2

| Bits | Spec Type | Default Value | Description |
|------|-----------|---------------|-------------|
| 31:0 |           | 0h            | N/A         |

[Table 140] VF BAR3

| Bits | Spec Type | Default Value | Description |
|------|-----------|---------------|-------------|
| 31:0 |           | 0h            | N/A         |

[Table 141] VF BAR4

| Bits | Spec Type | Default Value | Description |
|------|-----------|---------------|-------------|
| 31:0 |           | 0h            | N/A         |

[Table 142] VF BAR5

| Bits | Spec Type | Default Value | Description |
|------|-----------|---------------|-------------|
| 31:0 |           | 0h            | N/A         |

[Table 143] VF Migration State Array Offset

| Bits | Spec Type | Default Value | Description               |
|------|-----------|---------------|---------------------------|
| 31:3 |           | 0h            | VF Migration State Offset |
| 2:0  |           | 0h            | VF Migration State BIR    |

#### 5.1.4.8 Data Link Feature Extended Capability

[Table 144] Data Link Feature Extended Summary

| Start Address | End Address | Symbol | Description                                  |
|---------------|-------------|--------|----------------------------------------------|
| 3A4h          | 3A7h        |        | Data Link Feature Extended Capability Header |
| 3A8h          | 3ABh        |        | Data Link Feature Capabilities Register      |
| 3ACh          | 3AFh        |        | Data Link Feature Status Register            |

[Table 145] Data Link Feature Extended Capability Header

| Bits  | Spec Type | Default Value | Description                        |
|-------|-----------|---------------|------------------------------------|
| 31:20 | RO        | 0h            | Next Capability Offset             |
| 19:16 | RO        | 1h            | Capability Version                 |
| 15:0  | RO        | 25h           | PCI Express Extended Capability ID |

[Table 146] Data Link Feature Capabilities Register

| Bits  | Spec Type | Default Value | Description                         |
|-------|-----------|---------------|-------------------------------------|
| 31    | HwInit    | 1h            | Data Link Feature Exchange Enable   |
| 30:23 | RsvdP     | 0h            | Reserved                            |
| 22:1  | RsvdP     | 0h            | Reserved                            |
| 0     | HwInit    | 1h            | Local Scaled Flow Control Supported |

[Table 147] Data Link Feature Status Register

| Bits  | Spec Type | Default Value | Description                              |
|-------|-----------|---------------|------------------------------------------|
| 31    | RO        | 0h            | Remote Data Link Feature Supported Valid |
| 30:23 | RsvdP     | 0h            | Reserved                                 |
| 22:1  | RO        | 0h            | Undefined                                |
| 0     | RO        | 0h            | Remote Scaled Flow Control Supported     |

## 5.2 NVM Express Registers

### 5.2.1 Register Summary

[Table 148] Register Summary

| Start Address                         | End Address                           | Name     | Type                                     |
|---------------------------------------|---------------------------------------|----------|------------------------------------------|
| 00h                                   | 07h                                   | CAP      | Controller Capabilities                  |
| 08h                                   | 0Bh                                   | VS       | Version                                  |
| 0Ch                                   | 0Fh                                   | INTMS    | Interrupt Mask Set                       |
| 10h                                   | 13h                                   | INTMC    | Interrupt Mask Clear                     |
| 14h                                   | 17h                                   | CC       | Controller Configuration                 |
| 18h                                   | 1Bh                                   | Reserved | Reserved                                 |
| 1Ch                                   | 1Fh                                   | CSTS     | Controller Status                        |
| 20h                                   | 23h                                   | NSSR     | NVM Subsystem Reset (Optional)           |
| 24h                                   | 27h                                   | AQA      | Admin Queue Attributes                   |
| 28h                                   | 2Fh                                   | ASQ      | Admin Submission Queue Base Address      |
| 30h                                   | 37h                                   | ACQ      | Admin Completion Queue Base Address      |
| 38h                                   | EFFh                                  | Reserved | Reserved                                 |
| F00h                                  | FFFh                                  | Reserved | Command Set Specific                     |
| 1000h                                 | 1003h                                 | SQ0TDBL  | Submission Queue 0 Tail Doorbell (Admin) |
| 1000h + (1 * (4 << CAP.DSTRD))        | 1003h + (1 * (4 << CAP.DSTRD))        | CQ0TDBL  | Completion Queue 0 Head Doorbell (Admin) |
| ...                                   |                                       |          |                                          |
| 1000h+ (2y * (4 << CAP.DSTRD))        | 1003h + (2y * (4 << CAP.DSTRD))       | SQyTDBL  | Submission Queue y Tail Doorbell         |
| 1000h + ((2y + 1) * (4 << CAP.DSTRD)) | 1003h + ((2y + 1) * (4 << CAP.DSTRD)) | CQyHDBL  | Completion Queue y Head Doorbell         |

### 5.2.2 Controller Registers

[Table 149] Controller Capabilities

| Bits | Type | Name | Default Value | Description |
|------|------|------|---------------|-------------|
|------|------|------|---------------|-------------|

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|                   |    |        |                                               |                                                     |
|-------------------|----|--------|-----------------------------------------------|-----------------------------------------------------|
| 63:56             | RO | -      | 0h                                            | Reserved                                            |
| 55:52             | RO | MPSMAX | 01h                                           | Memory Page Size Maximum ((2 ^ (12 + MPSMAX)).      |
| 51:48             | RO | MPSMIN | 0                                             | Memory Page Size Minimum (2 ^ (12 + MPSMIN)).       |
| 47:45             | RO | -      | 0                                             | Reserved                                            |
| 44:37             | RO | CSS    | 1h                                            | Command Sets Supported<br>1h: NVM command set       |
| 36                | RO | NSSRS  | 1h                                            | NVM Subsystem Reset Supported (NSSRS)               |
| 35:32             | RO | DSTRD  | 0                                             | Doorbell Stride<br>0: Stride of 4 bytes             |
| 31:24             | RO | TO     | 50h (1.92TB, 3.84TB)<br>B4h (7.68TB, 15.36TB) | Timeout<br>(This field is in 500 millisecond units) |
| 23:19             | RO | -      | 0                                             | Reserved                                            |
| 18:17             | RO | AMS    | 1                                             | Arbitration Mechanism Supported                     |
| 16                | RO | CQR    | 1                                             | Contiguous Queues Required                          |
| 15:0              | RO | MQES   | 3FFh                                          | Maximum Queue Entries Supported                     |
| Offset 20h, 31:00 | RW | NSSRC  | 0h                                            | NVM Subsystem Reset Control (NSSRC)                 |

[Table 150] Version

| Bits  | Type | Name | Default Value | Description          |
|-------|------|------|---------------|----------------------|
| 31:16 | RO   | MJR  | 1h            | Major Version Number |
| 15:0  | RO   | MNR  | 30h           | Minor Version Number |

**NOTE:**

The PM1733 supports NVMe Express version 1.3

[Table 151] Interrupt Mask Set

| Bits  | Type | Name | Default Value | Description               |
|-------|------|------|---------------|---------------------------|
| 31:00 | RW1S | IVMS | 0             | Interrupt Vector Mask Set |

[Table 152] Interrupt Mask Clear

| Bits  | Type | Name | Default Value | Description                 |
|-------|------|------|---------------|-----------------------------|
| 31:00 | RW1C | IVMC | 0             | Interrupt Vector Mask Clear |

[Table 153] Controller Configuration

| Bits  | Type | Name   | Default Value | Description                                                                                                                                                                  |
|-------|------|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RO   | -      | 0             | Reserved                                                                                                                                                                     |
| 23:20 | RW   | IOCQES | 0             | I/O Completion Queue Entry Size<br>(Configured as a power of 2)<br>(Should be set to 4 for a 16 byte entry size)                                                             |
| 19:16 | RW   | IOSQES | 0             | I/O Submission Queue Entry Size<br>(Configured as a power of 2)<br>(Should be set to 6 for a 64 byte entry size)                                                             |
| 15:14 | RW   | SHN    | 0             | Shutdown Notification<br>0h: No notification<br>1h: Normal shutdown notification<br>2h: Abrupt shutdown notification<br>3h: Reserved<br>CSTS.SHST indicates shutdown status. |
| 13:11 | RW   | AMS    | 0             | Arbitration Mechanism Selected<br>0h: Round Robin<br>No other values supported.                                                                                              |
| 10:7  | RW   | MPS    | 0             | Memory Page Size<br>MPS is 2^(12+MPS)<br>Shall be within CAP.MPSMAX and CAP.MPSMIN ranges.                                                                                   |

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|     |    |     |   |                                                                                                                                                                                        |
|-----|----|-----|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:4 | RW | CSS | 0 | Command Set Selected<br>0h: NVM Command Set<br>No other values supported                                                                                                               |
| 3:1 | RO | -   | 0 | Reserved                                                                                                                                                                               |
| 0   | RW | EN  | 0 | Enable<br>When set to 1, controller shall process commands.<br>When cleared to 0, controller shall not process commands.<br>This field is subject to CSTS.RDY and CAP.TO restrictions. |

[Table 154] Controller Status

| Bits | Type | Name | Default Value | Description                                                                                                                                             |
|------|------|------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RO   | -    | 0             | Reserved                                                                                                                                                |
| 3:2  | RO   | SHST | 0             | Shutdown Status<br>0h: Normal operation, no shutdown requested<br>1h: Shutdown processing occurring<br>2h: Shutdown processing complete<br>3h: Reserved |
| 1    | RO   | CFS  | 0             | Controller Fatal Status                                                                                                                                 |
| 0    | RO   | RDY  | 0             | 1h: Controller ready to process commands<br>0h: Controller shall not process commands.                                                                  |

[Table 155] Admin Queue Attributes

| Bits  | Type | Name | Default Value | Description                                                                 |
|-------|------|------|---------------|-----------------------------------------------------------------------------|
| 31:28 | RO   | -    | 0             | Reserved                                                                    |
| 27:16 | RW   | ACQS | 0             | Admin Completion Queue Size<br>Max: 4096 (Value of 4095h - 0's based value) |
| 15:12 | RO   | -    | 0             | Reserved                                                                    |
| 11:0  | RW   | ASQS | 0             | Admin Submission Queue Size<br>Max: 4096 (Value of 4095h - 0's based value) |

[Table 156] Admin Submission Queue Base Address

| Bits  | Type | Name | Default Value | Description                         |
|-------|------|------|---------------|-------------------------------------|
| 63:12 | RW   | ASQB | 0             | Admin Submission Queue Base Address |
| 11:0  | RO   | -    | 0             | Reserved                            |

[Table 157] Admin Completion Queue Base Address

| Bits  | Type | Name | Default Value | Description                         |
|-------|------|------|---------------|-------------------------------------|
| 63:12 | RW   | ACQB | 0             | Admin Completion Queue Base Address |
| 11:0  | RO   | -    | 0             | Reserved                            |

[Table 158] Submission Queue Tail y Doorbell

| Bits  | Type | Name | Default Value | Description           |
|-------|------|------|---------------|-----------------------|
| 31:16 | RO   | -    | 0             | Reserved              |
| 15:0  | RW   | SQT  | 0             | Submission Queue Tail |

[Table 159] Completion Queue Head y Doorbell

| Bits  | Type | Name | Default Value | Description           |
|-------|------|------|---------------|-----------------------|
| 31:16 | RO   | -    | 0             | Reserved              |
| 15:0  | RW   | CQH  | 0             | Completion Queue Head |

## 6.0 SUPPORTED COMMAND SET

### 6.1 Admin Command Set

[Table 160] Opcode for Admin Commands

| Opcode (Hex) | Command Name                                                                                                                                                                                                                                                                                                                                                         |
|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00h          | Delete I/O Submission Queue                                                                                                                                                                                                                                                                                                                                          |
| 01h          | Create I/O Submission Queue                                                                                                                                                                                                                                                                                                                                          |
| 02h          | Get Log Page<br>- Error Information (01h)<br>- SMART/Health Information (02h)<br>- Firmware Slot Information (03h, M)                                                                                                                                                                                                                                                |
| 04h          | Delete I/O Completion Queue                                                                                                                                                                                                                                                                                                                                          |
| 05h          | Create I/O Completion Queue                                                                                                                                                                                                                                                                                                                                          |
| 06h          | Identify                                                                                                                                                                                                                                                                                                                                                             |
| 08h          | Abort                                                                                                                                                                                                                                                                                                                                                                |
| 09h          | Set Feature<br>- Arbitration (01h)<br>- Power Management (02h)<br>- LBA Range Type (03h)<br>- Temperature Threshold (04h)<br>- Error Recovery (05h)<br>- Number of Queues (07h)<br>- Interrupt Coalescing (08h)<br>- Interrupt Vector Configuration (09h)<br>- Write Atomicity (0Ah)<br>- Asynchronous Event Configuration (0Bh)<br>- Software Progress Marker (80h) |
| 0Ah          | Get Feature<br>- Arbitration (01h)<br>- LBA Range Type (03h)<br>- Temperature Threshold (04h)<br>- Error Recovery (05h)<br>- Number of Queues (07h)<br>- Interrupt Coalescing (08h)<br>- Interrupt Vector Configuration (09h)<br>- Write Atomicity (0Ah)<br>- Asynchronous Event Configuration (0Bh)<br>- Software Progress Marker (80h)                             |
| 0Ch          | Asynchronous Event Request                                                                                                                                                                                                                                                                                                                                           |
| 0Dh          | Namespace Management                                                                                                                                                                                                                                                                                                                                                 |
| 10h          | Firmware Commit                                                                                                                                                                                                                                                                                                                                                      |
| 11h          | Firmware Image Download                                                                                                                                                                                                                                                                                                                                              |
| 14h          | Device Self-test                                                                                                                                                                                                                                                                                                                                                     |
| 15h          | Namespace Attachment                                                                                                                                                                                                                                                                                                                                                 |
| 80h          | Format NVM                                                                                                                                                                                                                                                                                                                                                           |
| 81h - BFh    | I/O Command Set Specific                                                                                                                                                                                                                                                                                                                                             |

## 6.1.1 Identify Command

The Identify Command returns the data described below.

[Table 161] Identify Controller Data Structure

| Bytes   | O/M | Default Value                                                                                                                                             | Description                                                                                                                                  |
|---------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0     | M   | 144Dh                                                                                                                                                     | PCI Vendor ID                                                                                                                                |
| 3:2     | M   | 144Dh                                                                                                                                                     | PCI Subsystem Vendor ID                                                                                                                      |
| 23:4    | M   | SXXXXXXXXXXXXX                                                                                                                                            | Serial Number (ASCII), X: Variables                                                                                                          |
| 63:24   | M   | 1.92TB : SAMSUNG MZWLJ1T9HBJR-00007<br>3.84TB : SAMSUNG MZWLJ3T8HBLS-00007<br>7.68TB : SAMSUNG MZWLJ7T6HALA-00007<br>15.36TB : SAMSUNG MZWLJ15THALA-00007 | Model Number (ASCII)                                                                                                                         |
| 71:64   | M   | EPK9XB5Q                                                                                                                                                  | Firmware Revision, X: Variables                                                                                                              |
| 72      | M   | 8h                                                                                                                                                        | Recommended Arbitration Burst                                                                                                                |
| 75:73   | M   | 002538h                                                                                                                                                   | IEEE OUI<br>Byte 73 - 38h<br>Byte 74 - 25h<br>Byte 75 - 0h                                                                                   |
| 76      | O   | 3h                                                                                                                                                        | Controller Multi-Path I/O and<br>Namespace Sharing Capabilities (CMIC)                                                                       |
| 77      | M   | 5h                                                                                                                                                        | Maximum Data Transfer Size(MDTS)                                                                                                             |
| 79:78   | M   | 41h                                                                                                                                                       | Controller ID (CNTLID)                                                                                                                       |
| 83:80   | M   | 10300h                                                                                                                                                    | Version (VER)                                                                                                                                |
| 87:84   | M   | E4E1C0h (1.92TB, 3.84TB, 7.68TB)<br>C9C380h (15.36TB)                                                                                                     | RTD3 Resume Latency (RTD3R)                                                                                                                  |
| 91:88   | M   | 00989680h (1.92TB, 3.84TB, 7.68TB)<br>02625A00h (15.36TB)                                                                                                 | RTD3 Entry Latency (RTD3E)                                                                                                                   |
| 95:92   | M   | 300h                                                                                                                                                      | Optional Asynchronous Event Supported (OAES)                                                                                                 |
| 99:96   | M   | 0h                                                                                                                                                        | Controller Attributes (CTRATT)                                                                                                               |
| 239:100 |     | -                                                                                                                                                         | Reserved                                                                                                                                     |
| 255:240 |     | Refer to the NVMe Management Interface Specification for definition.                                                                                      |                                                                                                                                              |
| 257:256 | M   | DFh                                                                                                                                                       | Optional Admin Command Support                                                                                                               |
| 258     | M   | 7Fh                                                                                                                                                       | Abort Command Limit<br>(Maximum number of concurrently outstanding Abort<br>commands)<br>(0's based value)                                   |
| 259     | M   | Fh                                                                                                                                                        | Asynchronous Event Request Limit<br>(Maximum number of concurrently outstanding<br>Asynchronous Event Request commands)<br>(0's based value) |
| 260     | M   | 17h                                                                                                                                                       | Firmware Updates                                                                                                                             |
| 261     | M   | Eh                                                                                                                                                        | Log Page Attributes                                                                                                                          |
| 262     | M   | FFh                                                                                                                                                       | Error Log Page Entries<br>(Number of Error Information log entries stored by<br>controller)<br>(0's based value)                             |
| 263     | M   | 0h                                                                                                                                                        | Number of Power States Support<br>(0's based value)                                                                                          |
| 264     | M   | 1h                                                                                                                                                        | Admin Vendor Specific Command Configuration                                                                                                  |
| 265     | O   | 0h                                                                                                                                                        | Autonomous Power State Transition Attributes<br>(APSTA)                                                                                      |
| 267:266 | M   | 159h (1.92TB, 3.84TB, 7.68TB)<br>158h (15.36TB)                                                                                                           | Warning Composite Temperature Threshold<br>(WCTEMP)                                                                                          |

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## NVMe PCIe SSD

|                            |   |                                                                                                 |                                                   |
|----------------------------|---|-------------------------------------------------------------------------------------------------|---------------------------------------------------|
| 269:268                    | M | 166h (1.92TB, 3.84TB, 7.68TB)<br>165h (15.36TB)                                                 | Critical Composite Temperature Threshold (CCTEMP) |
| 271:270                    | O | 82h                                                                                             | Maximum Time for Firmware Activation (MTFA)       |
| 275:272                    | O | 0h                                                                                              | Host Memory Buffer Preferred Size (HMPRE):        |
| 279:276                    | O | 0h                                                                                              | Host Memory Buffer Minimum Size (HMMIN):          |
| 295:280                    | O | 1.92TB: 1BF1FC56000h<br>3.84TB: 37E3EE56000h<br>7.68TB : 6FC7D256000h<br>15.36TB : DF8F9A56000h | Total NVM Capacity (TNVMCAP):                     |
| 311:296                    | O | 0h                                                                                              | Unallocated NVM Capacity (UNVMCAP):               |
| 315:312                    | O | 0h                                                                                              | Replay Protected Memory Block Support (RPMBS):    |
| 317:316                    | O | 2h                                                                                              | Extended Device Self-test Time (EDSTT)            |
| 318                        | O | 1h                                                                                              | Device Self-test Options (DSTO)                   |
| 319                        | M | FFh                                                                                             | Firmware Update Granularity (FWUG)                |
| 321:320                    | M | 0h                                                                                              | Keep Alive Support(KAS)                           |
| 327:322                    | - | 0h                                                                                              | Reserved                                          |
| 331:328                    | O | 3h                                                                                              | Sanitize Capabilities (SANICAP)                   |
| 511:332                    | - | -                                                                                               | Reserved                                          |
| 512                        | M | 66h                                                                                             | Submission Queue Entry Size                       |
| 513                        | M | 44h                                                                                             | Completion Queue Entry Size                       |
| 515:514                    | - | -                                                                                               | Reserved                                          |
| 519:516                    | M | 20h                                                                                             | Number of Namespaces                              |
| 521:520                    | M | 7Fh                                                                                             | Optional NVM Command Support                      |
| 523:522                    | M | 0h                                                                                              | Fused Operation Support                           |
| 524                        | M | 4h                                                                                              | Format NVM Attributes                             |
| 525                        | M | 0h                                                                                              | Volatile Write Cache                              |
| 527:526                    | M | FFFFh                                                                                           | Atomic Write Unit Normal<br>All commands atomic   |
| 529:528                    | M | 0h                                                                                              | Atomic Write Unit Power Fail<br>(0's based value) |
| 530                        | M | 1h                                                                                              | NVM Vendor Specific Command Configuration         |
| 531                        | M | -                                                                                               | Reserved                                          |
| 533:532                    | O | 0h                                                                                              | Atomic Compare & Write Unit (ACWU)                |
| 535:534                    | M | -                                                                                               | Reserved                                          |
| 539:536                    | O | F0002h                                                                                          | SGL Support (SGLS)                                |
| 767:540                    | M | -                                                                                               | Reserved                                          |
| 1023:768                   | M | nqn.1994-11.com.samsung:nvme:<br>PM1733:2.5-inch:SXXXNXXXXXXXXXX                                | NVM Subsystem NVMe Qualified Name(SUBNQN)         |
| I/O Command Set Attributes |   |                                                                                                 |                                                   |
| 2047:1024                  | - | -                                                                                               | Reserved                                          |
| Power State Descriptors    |   |                                                                                                 |                                                   |
| 2079:2048                  | M | -                                                                                               | Power State 0 Descriptor                          |
| 2111:2080                  | O | -                                                                                               | Power State 1 Descriptor                          |
| 2143:2112                  | O |                                                                                                 | Power State 2 Descriptor                          |
| 2175:2144                  | O |                                                                                                 | Power State 3 Descriptor                          |

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|           |   |    |                                 |
|-----------|---|----|---------------------------------|
| 2207:2176 | O |    | Power State 4 Descriptor        |
| ...       | - |    |                                 |
| 3071:3040 | O | -  | Power State 31 Descriptor (N/A) |
| 4095:3072 | - | 0h | Samsung Reserved                |

[Table 162] Identify Power State Descriptor Data Structure

| Bits    | Default Value | Description                 |
|---------|---------------|-----------------------------|
| 255:184 | 0             | Reserved                    |
| 183:182 | 0             | Active Power Scale(APS)     |
| 181:179 | 0             | Reserved                    |
| 178:176 | 0             | Active Power Workload(APW)  |
| 175:160 | 0             | Active Power(ACTP)          |
| 159:152 | 0             | Reserved                    |
| 151:150 | 0             | Idle Power Scale(IPS)       |
| 149:144 | 0             | Reserved                    |
| 143:128 | 0             | Idle Power(IDLP)            |
| 127:125 | 0             | Reserved                    |
| 124:120 | 0             | Relative Write Latency      |
| 119:117 | 0             | Reserved                    |
| 116:112 | 0             | Relative Write Throughput   |
| 111:109 | 0             | Reserved                    |
| 108:104 | 0             | Relative Read Latency       |
| 103:101 | 0             | Reserved                    |
| 100:96  | 0             | Relative Read Throughput    |
| 95:64   | 0             | Exit Latency<br>(100us)     |
| 63:32   | 0             | Entry Latency<br>(100us)    |
| 31:26   | 0             | Reserved                    |
| 25      | 0             | Non-Operational State(NOPS) |
| 24      | 0             | Max Power Scale(MXPS)       |
| 23:16   | 0             | Reserved                    |
| 15:00   | 0             | Maximum Power               |

[Table 163] Identify Namespace Data Structure

| Bytes   | O/M | Default Value                                                                                   | Description                                                                                                                                                                                                                                                                                                                                                                                                    |
|---------|-----|-------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0     | M   | 1.92TB : DF8FE2B0h<br>3.84TB : 1BF1F72B0h<br>7.68TB : 37E3E92B0h<br>15.36TB : DF8F9A56h         | Namespace Size                                                                                                                                                                                                                                                                                                                                                                                                 |
| 15:8    | M   | 1.92TB : DF8FE2B0h<br>3.84TB : 1BF1F72B0h<br>7.68TB : 37E3E92B0h<br>15.36TB : DF8F9A56h         | Namespace Capacity                                                                                                                                                                                                                                                                                                                                                                                             |
| 23:16   | M   | 1.92TB : DF8FE2B0h<br>3.84TB : 1BF1F72B0h<br>7.68TB : 37E3E92B0h<br>15.36TB : DF8F9A56h         | Namespace Utilization                                                                                                                                                                                                                                                                                                                                                                                          |
| 24      | M   | 0h                                                                                              | Namespace Features<br>Bits 7:1 Reserved<br>Bit 0: Thin provisioning not supported                                                                                                                                                                                                                                                                                                                              |
| 25      | M   | 4h                                                                                              | Number of LBA Formats                                                                                                                                                                                                                                                                                                                                                                                          |
| 26      | M   | 10h                                                                                             | Formatted LBA Size<br>Bits 7:5 – Reserved<br>Bit 4: Metadata interleaved or separate (based on LBA format)<br>Bit 3:0 – Indicates LBA format                                                                                                                                                                                                                                                                   |
| 27      | M   | 3h                                                                                              | Metadata Capabilities<br>Bits 7:2 – Reserved<br>Bit 1 – Supports Metadata as separate buffer<br>Bit 0 – Supports Metadata as extended LBA                                                                                                                                                                                                                                                                      |
| 28      | M   | 1Fh                                                                                             | End-to-end Data Protection Capabilities<br>Bits 7:5 – Reserved<br>Bit 4 – Supports protection information as last 8 bytes of Metadata<br>Bit 3 – Supports protection information as first 8 bytes of Metadata<br>Bit 2 – Supports Type 3 protection information<br>Bit 1 – Supports Type 2 protection information<br>Bit 0 – Supports Type 1 protection information                                            |
| 29      | M   | 0h                                                                                              | End-to-End Data Protection Type Settings<br>Bits 7:4 – Reserved<br>Bit 3 – 1: Protection information transferred as first 8 bytes of Metadata<br>Bit 3 – 0: Protection information transferred as last 8 bytes of Metadata<br>Bit 2:0 – 000b: Protection information disabled<br>Bit 2:0 – 1h: Protection type 1 enabled<br>Bit 2:0 – 2h: Protection type 2 enabled<br>Bit 2:0 – 3h: Protection type 3 enabled |
| 30      | O   | 1h                                                                                              | Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC):                                                                                                                                                                                                                                                                                                                                            |
| 31      | O   | FFh                                                                                             | Reservation Capabilities (RESCAP):                                                                                                                                                                                                                                                                                                                                                                             |
| 32      | O   | 80h                                                                                             | Format Progress Indicator (FPI)                                                                                                                                                                                                                                                                                                                                                                                |
| 33      | O   | 1h                                                                                              | Deallocate Logical Block Features (DLFEAT):                                                                                                                                                                                                                                                                                                                                                                    |
| 35:34   | O   | 0h                                                                                              | Namespace Atomic Write Unit Normal (NAWUN)                                                                                                                                                                                                                                                                                                                                                                     |
| 37:36   | O   | 0h                                                                                              | Namespace Atomic Write Unit Power Fail (NAWUPF)                                                                                                                                                                                                                                                                                                                                                                |
| 39:38   | O   | 0h                                                                                              | Namespace Atomic Compare & Write Unit (NACWU)                                                                                                                                                                                                                                                                                                                                                                  |
| 41:40   | O   | 0h                                                                                              | Namespace Atomic Boundary Size Normal (NABSN)                                                                                                                                                                                                                                                                                                                                                                  |
| 43:42   | O   | 0h                                                                                              | Namespace Atomic Boundary Offset (NABO)                                                                                                                                                                                                                                                                                                                                                                        |
| 45:44   | O   | 0h                                                                                              | Namespace Atomic Boundary Size Power Fail (NABSPF)                                                                                                                                                                                                                                                                                                                                                             |
| 47:46   | -   | -                                                                                               | Reserved                                                                                                                                                                                                                                                                                                                                                                                                       |
| 63:48   |     | 1.92TB: 1BF1FC56000h<br>3.84TB: 37E3EE56000h<br>7.68TB : 6FC7D256000h<br>15.36TB : DF8F9A56000h | NVM Capacity (NVMCAP)                                                                                                                                                                                                                                                                                                                                                                                          |
| 103:64  | -   | -                                                                                               | Reserved                                                                                                                                                                                                                                                                                                                                                                                                       |
| 119:104 | O   | Device Dependant                                                                                | Namespace Globally Unique Identifier (NGUID)                                                                                                                                                                                                                                                                                                                                                                   |
| 127:120 | O   | 0h                                                                                              | IEEE Extended Unique Identifier(EUI64)                                                                                                                                                                                                                                                                                                                                                                         |
| 131:128 | M   | 1090000h                                                                                        | LBA Format 0 Support                                                                                                                                                                                                                                                                                                                                                                                           |

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|                 |   |           |                             |
|-----------------|---|-----------|-----------------------------|
| 135:132         | O | 3090008h  | LBA Format 1 Support        |
| 139:136         | O | C0000h    | LBA Format 2 Support        |
| 143:140         | O | 20C0008h  | LBA Format 3 Support        |
| 147:144         | O | 30C00040h | LBA Format 4 Support        |
|                 |   |           |                             |
| 191:188         | O | -         | LBA Format 15 Support (N/A) |
| 383:192         | - | -         | Reserved                    |
| Vendor Specific |   |           |                             |
| 4095:384        | - | -         | Samsung Reserved            |

[Table 164] LBA Format 0 Data Structure

| Bits  | Name  | Default Value | Description          |
|-------|-------|---------------|----------------------|
| 31:26 |       | 0h            | Reserved             |
| 25:24 | RP    | 1h            | Relative Performance |
| 23:16 | LBADS | 9h            | LBA Data Size        |
| 15:00 | MS    | 0h            | Metadata Size        |

[Table 165] LBA Format 1 Data Structure

| Bits  | Name  | Default Value | Description          |
|-------|-------|---------------|----------------------|
| 31:26 |       | 0h            | Reserved             |
| 25:24 | RP    | 3h            | Relative Performance |
| 23:16 | LBADS | 9h            | LBA Data Size        |
| 15:00 | MS    | 8h            | Metadata Size        |

[Table 166] LBA Format 2 Data Structure

| Bits  | Name  | Default Value | Description          |
|-------|-------|---------------|----------------------|
| 31:26 |       | 0             | Reserved             |
| 25:24 | RP    | 0h            | Relative Performance |
| 23:16 | LBADS | Ch            | LBA Data Size        |
| 15:00 | MS    | 0h            | Metadata Size        |

[Table 167] LBA Format 3 Data Structure

| Bits  | Name  | Default Value | Description                          |
|-------|-------|---------------|--------------------------------------|
| 31:26 |       | 0             | Reserved                             |
| 25:24 | RP    | 2h            | Relative Performance                 |
| 23:16 | LBADS | Ch            | LBA Data Size (2 <sup>n</sup> bytes) |
| 15:00 | MS    | 8h            | Metadata Size (bytes)                |

[Table 168] LBA Format 4 Data Structure

| Bits  | Name  | Default Value | Description                          |
|-------|-------|---------------|--------------------------------------|
| 31:26 |       | 0             | Reserved                             |
| 25:24 | RP    | 3h            | Relative Performance                 |
| 23:16 | LBADS | Ch            | LBA Data Size (2 <sup>n</sup> bytes) |
| 15:00 | MS    | 40h           | Metadata Size (bytes)                |

## 6.2 NVMe Express I/O Command Set

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datasheet

NVMe PCIe SSD

[Table 169] Opcode for NVMe Express I/O Commands

| Opcode (Hex) | Command Name         |
|--------------|----------------------|
| 00h          | Flush                |
| 01h          | Write                |
| 02h          | Read                 |
| 04h          | Write Uncorrectable  |
| 05h          | Write Zeroes         |
| 09h          | Dataset Management   |
| 0Dh          | Reservation Register |
| 0Eh          | Reservation Report   |
| 11h          | Reservation Acquire  |
| 15h          | Reservation Release  |

NOTE:  
1) Deallocate feature in Dataset Management command is only supported in the Samsung SSD PM1733.

## 7.0 SFF-8639 SMBus RESOURCES

This section listed data structures and registers accessible through SMBus interface.

Vital Product Data (VPD) is stored in SM-Bus slave address of 0xA6 (bits 7-1 correspond to 1010\_011 on the SM-Bus). Temperature sensor is stored in SM-Bus slave address of 0xD4 (bits 7-1 correspond to 1101\_010).

### 7.1 Vital Product Data (VPD) Structure

Data offset of VPD EEPROM is 1Byte(8bit).

VPD listed device specific information for Enterprise PCIe SSD discovery and power allocation.

| Bytes   | Name                       | Default Value                                                                                                                                                 | Description                                                                       |
|---------|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|
| 02:00   | Class Code                 | 010802h                                                                                                                                                       | Device Type & Programming Interface                                               |
| 04:03   | ID                         | 144Dh                                                                                                                                                         | PCI-SIG Vendor ID                                                                 |
| 24:05   | Serial Number              | SXXXNXXXXXXXXX                                                                                                                                                | Serial Number (Vendor Unique, ASCII String), X: Variables                         |
| 64:25   | Model Number               | 1.9TB: SAMSUNG<br>MZWLJ1T9HBJR-00007<br>3.8TB: SAMSUNG<br>MZWLJ3T8HBLs-00007<br>7.6TB: SAMSUNG<br>MZWLJ7T6HALA-00007<br>15.2TB: SAMSUNG<br>MZWLJ15THALA-00007 | Model Number (ASCII String)                                                       |
| 65:65   | PCIe Port 0 Capabilities   | 04h                                                                                                                                                           | Maximum Link Speed (PCIe Gen4)                                                    |
| 66:66   | PCIe Port 0 Capabilities   | 04h                                                                                                                                                           | Maximum Link Width (x8)                                                           |
| 67:67   | PCIe Port 1 Capabilities   | 04h                                                                                                                                                           | Maximum Link Speed (PCIe Gen4)                                                    |
| 68:68   | PCIe Port 1 Capabilities   | 04h                                                                                                                                                           | Maximum Link Width (x8)                                                           |
| 69:69   | Initial Power Requirements | 1.92/3.84/7.68TB : 07h<br>15.36TB : 08h                                                                                                                       | 12V Power rail initial power requirement<br>(1.92/3.84/7.68TB : 7W, 15.36TB : 8W) |
| 71:70   | Initial Power Requirements | 0h                                                                                                                                                            | Reserved                                                                          |
| 72:72   | Max power Requirement      | 19h                                                                                                                                                           | 12V Power rail maximum power requirement (25W)                                    |
| 74:73   | Max power Requirement      | 0h                                                                                                                                                            | Reserved                                                                          |
| 76:75   | Cap List Pointer           | 0050h                                                                                                                                                         | Start Cap Address Pointer (0x50)                                                  |
| 79:77   | -                          | 0h                                                                                                                                                            | -                                                                                 |
| 81:80   | -                          | 00A2h                                                                                                                                                         | VU Cap ID                                                                         |
| 83:82   | -                          | 0070h                                                                                                                                                         | Next Cap Address (0x0070 VU Samsung Specific)                                     |
| 84:84   | Sensor Type                | 00h                                                                                                                                                           | -                                                                                 |
| 85:85   | Sensor Address             | 36h                                                                                                                                                           | -                                                                                 |
| 87:86   | -                          | 0h                                                                                                                                                            | Reserved                                                                          |
| 89:88   | Warning Thresh             | 1.92/3.84/7.68TB : 0480h<br>15.36TB : 0470h                                                                                                                   | 1.92/3.84/7.68TB : 72 Degree Celsius<br>15.36TB : 71 Degree Celsius               |
| 91:90   | OverTemp Thresh            | 1.92/3.84/7.68TB : 0550h<br>15.36TB : 0540h                                                                                                                   | 1.92/3.84/7.68TB : 85 Degree Celsius<br>15.36TB : 84 Degree Celsius               |
| 92:92   | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 93:93   | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 94:94   | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 95:95   | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 96:96   | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 97:97   | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 98:98   | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 99:99   | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 100:100 | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 101:101 | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 102:102 | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 103:103 | -                          | FFh                                                                                                                                                           | Reserved                                                                          |
| 104:104 | -                          | FFh                                                                                                                                                           | Reserved                                                                          |

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|         |   |       |                                                          |
|---------|---|-------|----------------------------------------------------------|
| 105:105 | - | FFh   | Reserved                                                 |
| 106:160 | - | FFh   | Reserved                                                 |
| 107:107 | - | FFh   | Reserved                                                 |
| 108:108 | - | FFh   | Reserved                                                 |
| 109:109 | - | FFh   | Reserved                                                 |
| 110:110 | - | FFh   | Reserved                                                 |
| 111:111 | - | FFh   | Reserved                                                 |
| 113:112 | - | 00A0h | Dual Port Mode Capability                                |
| 115:114 | - | 0074h | Next Cap Address (0x0074 Dual Active/Passive Capability) |
| 117:116 | - | 00A3h | Dual Active/Passive Capability                           |
| 119:118 | - | 0000h | Next Cap Address (NULL)                                  |
| 120:120 | - | 03h   | Dual Port Vector (Dual Port Passive)                     |
| 121:121 | - | 00h   | Reserved                                                 |
| 122:122 | - | 00h   | Reserved                                                 |
| 123:123 | - | 00h   | Reserved                                                 |
| 255:124 | - | FFh   | Reserved                                                 |

**NOTE:** TSE2004av temperature encoding:

| B15/B07 | B14/B06 | B13/B05 | B12/B04 | B11/B03 | B10/B02 | B09/B01 | B08/B00 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| N/A     | N/A     | N/A     | Sign    | 128     | 64      | 32      | 16      |
| 8       | 4       | 2       | 1       | N/A     | N/A     | N/A     | N/A     |

The 16-bit value is 2s complement representation of a temperature with the Bit 4 equal to the minimum granularity of 1 °C. Bit 12 is the sign bit.

For example:

1. a value of 0190h represents 25 °C,
2. a value of 07C0 h represents 124 °C, and
3. a value of 1E80 h represents –24 °C

By choosing the starting of the lowest bit the resolution of the temperature sensor can be defined. For SMBus temperature capability support PM1725's temperature sensor is at resolution of 1°C (8-bit)

## 7.2 Temperature Sensor Register Summary

| Offset | Type | Name                | Description                              | Default |
|--------|------|---------------------|------------------------------------------|---------|
| 00     | RO   | Capabilities        | Indicates the functions and capabilities | 00EFh   |
| 01     | RW   | Configuration       | Temperature sensor control               | 0000h   |
| 02     | RW   | High Limit          | Temperature High Limit                   | 0000h   |
| 03     | RW   | Low Limit           | Temperature Low Limit                    | 0000h   |
| 04     | RW   | TCRIT Limit         | Critical Temperature                     | 0000h   |
| 05     | RO   | Ambient Temp        | Current Ambient Temperature              | N/A     |
| 06     | RO   | Manufacture ID      | PCI-SIG Manufacture ID                   | 1C85h   |
| 07     | RO   | Device/Revision     | Device ID and Revision number            | 2221h   |
| 08     | RW   | Resolution register | Sets temperature resolution              | 0001h   |

## 7.2.1 Capabilities Register

| Bits  | Type | Default Value | Description                                                                                                                                                                                                                                                                                                                                        |
|-------|------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:08 | RO   | 0             | Reserved                                                                                                                                                                                                                                                                                                                                           |
| 7     | RO   | 1             | Event output status during Shutdown (SHDN Status):<br>0 = Event output remains in previous state. If the output asserts before shutdown command, it remains asserted during shutdown.<br>1 = Event output deasserts during shutdown. After shutdown, it takes tCONV to re-assert the Event output (default)                                        |
| 6     | RO   | 1             | Bus timeout period access during normal operation.<br>0 = Bus time-out range is 10 ms to 60 ms<br>1 = Bus time-out range is 25 ms to 35 ms (default)                                                                                                                                                                                               |
| 5     | RO   | 1             | Support SA0 high level input voltage (VHV) for SA0 pin.<br>0 = Pin A0 does not accept High Voltage<br>1 = Pin A0 accepts High Voltage for the EEPROM Write Protect feature (default)                                                                                                                                                               |
| 04:03 | RO   | 1             | Indicates the temperature resolution. Temperature resolution is set on the resolution register.<br>00 : 9-bit temperature resolution (0.5°C resolution)<br>01 : 10-bit temperature resolution (0.25°C resolution) (default)<br>10 : 11-bit temperature resolution (0.125°C resolution)<br>11 : 12-bit temperature resolution (0.0625°C resolution) |
| 2     | RO   | 1             | Range Width:<br>0 : TA=0 (decimal) for temperature below 0°C<br>1 : The part can measure temperature below 0°C (default)                                                                                                                                                                                                                           |
| 1     | RO   | 1             | Accuracy:<br>0 = Accuracy $\pm 2^{\circ}\text{C}$ over the active range and $\pm 3^{\circ}\text{C}$ over the monitoring range (C-grade).<br>1 = High accuracy $\pm 1^{\circ}\text{C}$ over the active range and $\pm 2^{\circ}\text{C}$ over the monitoring range (B-grade) (default)                                                              |
| 0     | RO   | 1             | Temperature Alarm:<br>0 = No defined function (This bit will never be cleared or set to '0'.)<br>1 = The part has temperature boundary trip limits (TUPPER/TLOWER/TCRIT registers) and a temperature event output (default, JC 42.4 required feature)                                                                                              |

### 7.2.2 Configuration Register

| Bits  | Type | Default Value | Description                                                                                                                                                                                 |
|-------|------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RW   | 0             | Reserved                                                                                                                                                                                    |
| 10:09 | RW   | 0             | TUPPER and TLOWER Limit Hysteresis (THYST):<br>00 = 0°C (default)<br>01 = 1.5°C<br>10 = 3.0°C<br>11 = 6.0°C                                                                                 |
| 08    | RW   | 0             | Shutdown Mode (SHDN):<br>0 = Continuous Conversion (default)<br>1 = Shutdown (Low-Power mode)                                                                                               |
| 07    | RW   | 0             | TCRIT Lock Bit (Crit. Lock):<br>0 = Unlocked. TCRIT register can be written (default)<br>1 = Locked. TCRIT register can not be written                                                      |
| 06    | RW   | 0             | TUPPER and TLOWER Window Lock Bit (Win. Lock):<br>0 = Unlocked. TUPPER and TLOWER registers can be written (default)<br>1 = Locked. TUPPER and TLOWER registers can not be written          |
| 05    | RW   | 0             | Interrupt Clear (Int. Clear) Bit:<br>0 = No effect (default)<br>1 = Clear interrupt output. When read this bit returns '0'                                                                  |
| 04    | RW   | 0             | Event Output Status (Event Stat.) Bit:<br>0 = Event output is not asserted by the device (default)<br>1 = Event output is asserted as a comparator/Interrupt or critical temperature output |
| 03    | RW   | 0             | Event Output Control (Event Cnt.) Bit:<br>0 = Event output Disabled (default)<br>1 = Event output Enabled                                                                                   |
| 02    | RW   | 0             | Event Output Select (Event Sel.) Bit:<br>0 = Event output for TUPPER, TLOWER and TCRIT (default)<br>1 = TA ≥ TCRIT only. (TUPPER and TLOWER temperature boundaries are disabled.)           |
| 01    | RW   | 0             | Event Output Polarity (Event Pol.) Bit:<br>0 = Active low (default. Pull-up resistor required)<br>1 = Active-high                                                                           |
| 00    | RW   | 0             | Event Output Mode (Event Mod.) Bit:<br>0 = Comparator output (default)<br>1 = Interrupt output                                                                                              |

### 7.2.3 High Limit Register

| Bits  | Type | Default Value | Description                 |
|-------|------|---------------|-----------------------------|
| 15:13 | RW   | 0             | Reserved                    |
| 12    | RW   | 0             | Sign bit of the temperature |
| 11    | RW   | 0             | 128 degree celsius          |
| 10    | RW   | 0             | 64 degree celsius           |
| 09    | RW   | 0             | 32 degree celsius           |
| 08    | RW   | 0             | 16 degree celsius           |
| 07    | RW   | 0             | 8 degree celsius            |
| 06    | RW   | 0             | 4 degree celsius            |
| 05    | RW   | 0             | 2 degree celsius            |
| 04    | RW   | 0             | 1 degree celsius            |
| 03:00 | RW   | 0             | Reserved                    |

#### 7.2.4 Low Limit Register

| Bits  | Type | Default Value | Description                 |
|-------|------|---------------|-----------------------------|
| 15:13 | RW   | 0             | Reserved                    |
| 12    | RW   | 0             | Sign bit of the temperature |
| 11    | RW   | 0             | 128 degree celsius          |
| 10    | RW   | 0             | 64 degree celsius           |
| 09    | RW   | 0             | 32 degree celsius           |
| 08    | RW   | 0             | 16 degree celsius           |
| 07    | RW   | 0             | 8 degree celsius            |
| 06    | RW   | 0             | 4 degree celsius            |
| 05    | RW   | 0             | 2 degree celsius            |
| 04    | RW   | 0             | 1 degree celsius            |
| 03:00 | RW   | 0             | Reserved                    |

#### 7.2.5 Critical Temperature Register

| Bits  | Type | Default Value | Description                 |
|-------|------|---------------|-----------------------------|
| 15:13 | RW   | 0             | Reserved                    |
| 12    | RW   | 0             | Sign bit of the temperature |
| 11    | RW   | 0             | 128 degree celsius          |
| 10    | RW   | 0             | 64 degree celsius           |
| 09    | RW   | 0             | 32 degree celsius           |
| 08    | RW   | 0             | 16 degree celsius           |
| 07    | RW   | 0             | 8 degree celsius            |
| 06    | RW   | 0             | 4 degree celsius            |
| 05    | RW   | 0             | 2 degree celsius            |
| 04    | RW   | 0             | 1 degree celsius            |
| 03:00 | RW   | 0             | Reserved                    |

#### 7.2.6 Ambient Temperature Register

| Bits  | Type | Default Value | Description                                           |
|-------|------|---------------|-------------------------------------------------------|
| 15    | RO   | 0             | TCRIT Flag: The temperature is above the TCRIT Limit. |
| 14    | RO   | 0             | High Flag: The temperature is above the High Limit.   |
| 13    | RO   | 0             | Low Flag: The temperature is below the Low Limit.     |
| 12    | RO   | 0             | Sign bit of the temperature                           |
| 11    | RO   | 0             | 128 degree celsius                                    |
| 10    | RO   | 0             | 64 degree celsius                                     |
| 09    | RO   | 0             | 32 degree celsius                                     |
| 08    | RO   | 0             | 16 degree celsius                                     |
| 07    | RO   | 0             | 8 degree celsius                                      |
| 06    | RO   | 0             | 4 degree celsius                                      |
| 05    | RO   | 0             | 2 degree celsius                                      |
| 04    | RO   | 0             | 1 degree celsius                                      |
| 03:00 | RO   | 0             | Reserved                                              |

### 7.2.7 Manufacture ID Register

| Bits | Type | Default Value | Description            |
|------|------|---------------|------------------------|
| 15:0 | RO   | 144Dh         | PCI-SIG Manufacture ID |

### 7.2.8 Device/Revision Register

| Bits | Type | Default Value | Description                   |
|------|------|---------------|-------------------------------|
| 15:0 | RO   | 0xA824        | Device ID and Revision Number |

### 7.2.9 Resolution Register

| Bits  | Type | Default Value | Description                                                                                                                                                                                                 |
|-------|------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:02 | RW   | 00            | Reserved                                                                                                                                                                                                    |
| 01:00 | RW   | 01            | Resolution:<br>00 = LSB = 0.5°C (tCONV = 23 ms typical)<br>01 = LSB = 0.25°C (default, tCONV = 46 ms typical)<br>10 = LSB = 0.125°C (tCONV = 75 ms typical)<br>11 = LSB = 0.0625°C (tCONV = 150 ms typical) |

## 8.0 PRODUCT COMPLIANCE

### 8.1 Product Regulatory Compliance and Certifications

| Category | Certifications          |
|----------|-------------------------|
| Safety   | cUL                     |
|          | CE                      |
|          | TUV-GS                  |
|          | CB                      |
| EMC      | CE (EU)                 |
|          | BSMI (Taiwan)           |
|          | KC (South Korea)        |
|          | VCCI (Japan)            |
|          | RCM (Australia)         |
|          | FCC (USA) / IC (Canada) |

The three existing compliance marks (C-Tick, A-Tick, and RCM) are consolidated into a single compliance mark - the RCM.



Caution: Any changes or modifications in construction of this device which are not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### NOTE:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio / TV technician for help.

Modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment under FCC rules.



- 1.기자재 명칭 : SSD (Solid State Drive)
- 2.모델명(Model): 라벨 별도 표기
- 3.제조연월 : 라벨 별도 표기
- 4.제조사 : 삼성전자(주)
- 5.제조국가 : 대한민국
- 6.상호명 : 삼성전자(주)

#### Industry Canada ICES-003 Compliance Label:

CAN ICES-3 (B)/NMB-3(B)

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## 9.0 REFERENCES

[Table 170] Standards References

| Item                                                                | Website                                                                                                                     |
|---------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| PCI Express Base Specification Revision 4.0                         | <a href="http://www.pcisig.com/specifications/">http://www.pcisig.com/specifications/</a>                                   |
| NVM Express Specification Rev. 1.3                                  | <a href="http://www.nvmexpress.org/">http://www.nvmexpress.org/</a>                                                         |
| NVMe Management Interface 1.0a                                      | <a href="http://www.nvmexpress.org/">http://www.nvmexpress.org/</a>                                                         |
| Enterprise SSD Form Factor Version 1.0a                             | <a href="http://www.ssdformfactor.org/">http://www.ssdformfactor.org/</a>                                                   |
| Solid-State Drive Requirements and Endurance Test Method (JESD218A) | <a href="http://www.jedec.org/standards-documents/docs/jesd218a">http://www.jedec.org/standards-documents/docs/jesd218a</a> |
| Solid-State Drive Requirements and Endurance Test Method (JESD219A) | <a href="http://www.jedec.org/standards-documents/docs/jesd219a">http://www.jedec.org/standards-documents/docs/jesd219a</a> |